

Quad D-Type Flip-Flop Logic IC with Reset in bare die form

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Description

The 54HC175 is fabricated using a 2.5µm 5V CMOS process and consists of four D-Type flip–flops each with separate D input and common Reset and Clock inputs. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Reset is clock independent and is accomplished by a low level on the Reset line. The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

Ordering Information

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection
 + MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

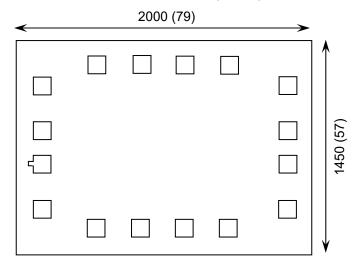
Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Features:

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Low Input Current: 1µA
- High Noise Immunity Characteristics of CMOS
- Operating Voltage Range: 2.0 to 6.0 V
- Direct drop-in replacement for obsolete components in long term programs.

Die Dimensions in µm (mils)



Mechanical Specification

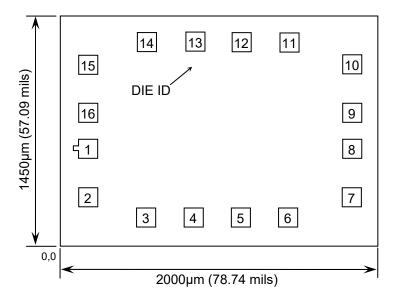
Die Size (Unsawn)	2000 x 1450 79 x 57	μm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	μm mils
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1μ	m
Back Metal Composition	N/A – Bare S	Si



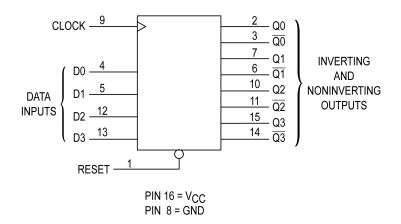


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Pad Layout and Functions



Logic Diagram



PAD	FUNCTION	COORDINA	ATES (mm)	
FAD	TONCTION	X	Y	
1	RESET	0.122	0.554	
2	Q0	0.122	0.251	
3	Q0	0.480	0.122	
4	D0	0.780	0.122	
5	D1	1.070	0.122	
6	Q1	1.370	0.122	
7	Q1	1.771	0.251	
8	GND	1.771	0.554	
9	CLOCK 1.771		0.781	
10	Q2	1.771	1.084	
11	Q2 1.373		1.222	
12	D2	1.073	1.222	
13	D3	0.783	1.222	
14	Q3	0.483	1.222	
15	Q3	0.122	1.084	
16	V _{CC}	0.122	0.781	
CON	NECT CHIP BA	CK TO V _{CC} C	R FLOAT	

Truth Table

I	NPUTS	OUTP	UTS	
RESET	CLOCK	D	Q	Q
L	Х	Χ	L	Н
Н		Н	Н	L
Н		L	L	Н
Н	L	Χ	No Cl	nange





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-1.5 to V _{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
Storage Temperature Range	T _{STG}	-65 to 150	°C
Input Current (per Pad)	I _{IN}	±20	mA
Output Current (per Pad)	I _{OUT}	±25	mA
DC Supply Current, V _{CC} or GND, per pad	I _{cc}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

		0			•
PARAMETE	SYMBOL	MIN	MAX	UNITS	
Supply Voltage		V _{CC}	2.0	6.0	V
DC Input Voltage, Outp	$V_{IN,}V_{OUT}$	0	V _{CC}	V	
Operating Temperature Range		T _J	-55	+125	°C
Input Rise / Fall Time V_{CC} =2.0V V_{CC} =4.5V V_{CC} =6.0V			0	1000	
		t _r , t _f	0	500	ns
			0	400	

^{3.} This device contains protection circuitry against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of voltage higher than max rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to range GND \leq (V_{IN} or V_{OUT}) \leq V_{CC} . Unused inputs must be tied to an appropriate logic voltage level (e.g., GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER SYMBOL	SYMBOL	V _{cc}	CONDITIONS		UNITS		
	OTHIBOL	• 66	CONDITIONS	25°C	85°C	FULL RANGE⁴	Oitilo
Minima una Iliada I aval		2.0	V _{OUT} = 0.1V	1.5	1.5	1.5	
Minimum High-Level Input Voltage	V _{IH}	4.5	or V _{CC} -0.1V	3.15	3.15	3.15	V
input voltage		6.0	I _{OUT} ≤ 20μA	4.2	4.2	4.2	
Maximum Low-Level V		2.0	$V_{OUT} = 0.1V$ or V_{CC} -0.1V $\left I_{OUT} \right \le 20\mu A$	0.3	0.3	0.3	
	V _{IL}	4.5		0.9	0.9	0.9	V
put t citage		6.0		1.2	1.2	1.2	
		2.0	\/ =\/ a=\/	1.9	1.9	1.9	
		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	4.4	4.4	4.4	V
Minimum High-Level		6.0		5.9	5.9	5.9	
Output Voltage	V _{OH} 4.5	4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	3.98	3.84	3.7	V
		6.0	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	5.48	5.34	5.2	V





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DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER SYMBO	SYMBOL	V _{cc} CONDITIONS	CONDITIONS		UNITS			
	OTHEOL		25°C	85°C	FULL RANGE⁴	Oitilo		
		2.0	\/ =\/ or\/	0.1	0.1	0.1		
	V _{OL}	4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	0.1	0.1	0.1	V	
Maximum Low-Level		6.0	0.1	0.1	0.1			
Output Voltage		V _{OL}	4.5	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	0.26	0.33	0.4	V
					6.0	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	0.26	0.33
Maximum Input Leakage Current	I _{IN}	6.0	V _{IN} = GND or V _{CC}	±0.1	±1.0	±1.0	μА	
Maximum Quiescent Supply Current	I _{CC}	6.0	V_{IN} = GND or V_{DD} I_{OUT} = 0μ A	8	80	160	μА	

⁴. -55°C ≤ T_J ≤ +125°C

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIMIT	rs	UNITS
i / u o une i en	STWIDOL	VCC SOMETHIONS	25°C	85°C	FULL RANGE⁴	ONITS	
Maximum Clock		2.0	0 - 50-5	6.0	4.8	4.0	
Frequency	f _{max}	4.5	$C_L = 50pF,$ $t_r = t_f = 6ns$	30	24	20	MHz
(Figure 1, 4)		6.0	प प जाठ	35	28	24	
Propagation Delay,		2.0	2.0 4.5 $t_r = t_f = 6 \text{ns}$	150	190	225	
Clock to Q or Q	t _{PLH} , t _{PHL}	4.5		30	38	45	ns
(Figure 1, 4)		6.0		26	33	38	
Propagation Delay,		2.0	C - 50°5	125	155	190	
Reset to Q or Q t _{PLH} , t _{PHL}	t _{PLH} , t _{PHL}	4.5	$C_L = 50pF,$ $t_r = t_f = 6ns$	25	31	38	ns
(Figure 2, 4)		6.0	ų ų one	21	26	32	
Output Transition		2.0	C = 50pF	75	95	110	
Time, Any Output	t _{TLH} , t _{THL}	4.5	$C_L = 50pF,$ $t_r = t_f = 6ns$	15	19	22	ns
(Figure 1, 4)		6.0	ų ų 0.1.5	13	16	19	
Input Capacitance	C _{IN}	-	$C_L = 50pF,$ $t_r = t_f = 6ns$	10	10	10	pF
Power Dissipation Capacitance	C _{PD}	_	T _J = 25°C, V _{CC} = 5.0V		TYPIC	AL	pF
(Per Flip-Flop)	ОРО	V _{cc}			35		Pi

^{5.} Not production tested in die form, characterized by chip design and tested in package.





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Timing Requirements⁵

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIMIT	S	UNITS
. ,	OTMIDGE	TCC GONDINON	CONDITIONS	25°C	85°C	FULL RANGE⁴	
Minimum Setup Time, Data to Clock (Figure 3)		2.0	$C_L = 50pF,$ $t_r = t_f = 6ns$	100	125	150	
	t _{su}	4.5		20	25	30	ns
		6.0	ų ų 0.15	17	21	26	
Minimum Hold Time,		2.0	C _L = 50pF,	3.0	3.0	3.0	
Clock to Data	t _h	4.5	$t_r = t_f = 6$ ns	3.0	3.0	3.0	ns
(Figure 3)		6.0		3.0	3.0	3.0	
Minimum Recovery Time, Reset Inactive		2.0	$C_L = 50 pF,$ $t_r = t_f = 6 ns$	100	125	150	ns
	t _{rec}	4.5		20	25	30	
to Clock (Figure 2)		6.0		17	21	26	
Minimum Pulse		2.0	C = 50pF	80	100	120	
Width, Clock	t _w	4.5	$C_L = 50pF,$ $t_r = t_f = 6ns$	16	20	24	ns
(Figure 1)		6.0	_г – _г – опз	14	17	20	
Minimum Pulse		2.0	C _L = 50pF,	80	100	120	
Width, Reset	t _w	t _w 4.5	$t_r = t_f = 6$ ns	16	20	24	ns
(Figure 2)		6.0	1 1 -	14	17	20	
Maximum Input Rise		2.0	C = 50pF	1000	1000	1000	
and Fall Times	t _r , t _f	4.5	$C_L = 50pF,$ $t_r = t_f = 6ns$	500	500	500	ns
(Figure 1)	Ī	6.0	4 4 55	400	400	400	

⁵. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveforms

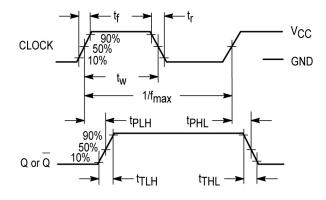


Figure 1 – Data, Clock and Output

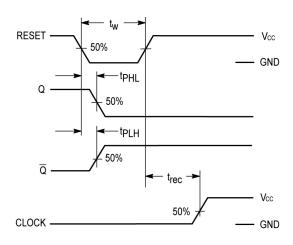


Figure 2 – Reset, Clock and Output





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Switching Waveforms continued

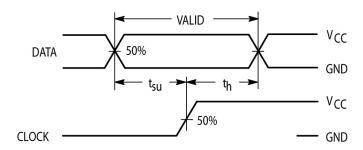
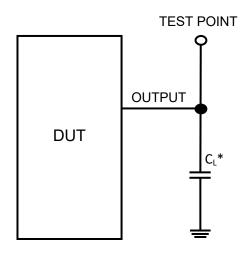


Figure 3 - Clock to Data



* Includes all probe and jig capacitance

Figure 4 – Test Circuit

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