High Speed CMOS Logic – 54HC164

8-Bit Serial-Input / Parallel-Output Shift Register in bare die form

Rev 1.0
24/11/17

Description

The 54HC164 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. The device consists of x2 serial data inputs, A and B, provided so that one input can be used as a data enable. Data is entered on each rising edge of the clock. A LOW on the master reset input ($\overline{CLR}$) clears the register, forcing all outputs LOW, independent of other inputs. Inputs are compatible with standard CMOS outputs and LSTTL via use of pull-up resistors. All inputs are equipped with protection circuits against static discharge & transient excess voltage.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS164
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

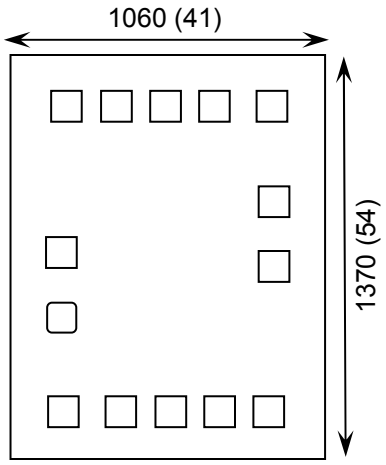
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1060 x 1370 41 x 54	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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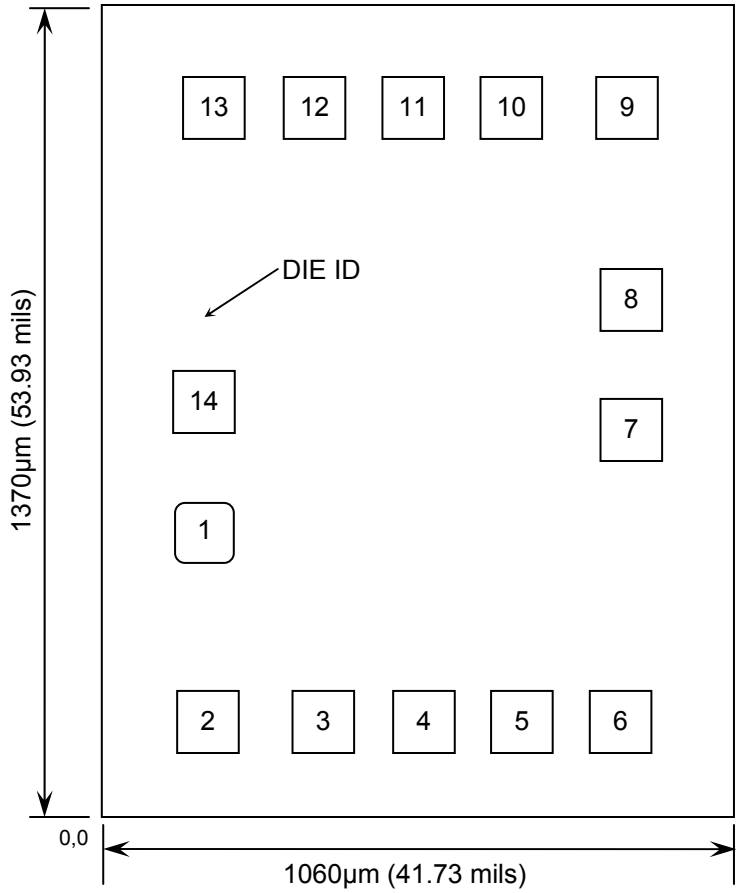
Pad Layout and Functions



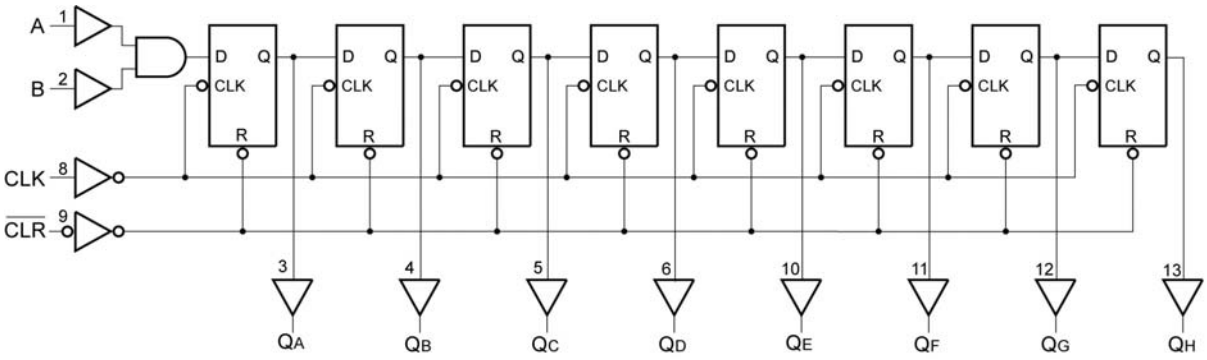
PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.117	0.439
2	B	0.124	0.115
3	Q_A	0.3195	0.115
4	Q_B	0.4875	0.115
5	Q_C	0.6555	0.115
6	Q_D	0.8235	0.115
7	GND	0.841	0.61
8	CLK	0.841	0.831
9	$\overline{CLR}$	0.833	1.155
10	Q_E	0.6385	1.155
11	Q_F	0.4705	1.155
12	Q_G	0.3025	1.155
13	Q_H	0.1345	1.155
14	V_{CC}	0.117	0.662
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Function Table

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	… Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{Gn}

D = Data Input
Q_{An} - Q_{Gn} = Data shift from preceding register on rising edge clock input

Logic Diagram



Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Input Rise and Fall Time	V_{CC} = 2.0V	t_r, t_f	0	1000	Ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	1.5	1.5	1.5	V
		3V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20μA	0.5	0.5	0.5	V
		3V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

4. -55˚C ≤ T_J ≤ +125˚C

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 2.4mA$	2.48	2.34	2.20	V
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	3.98	3.84	3.70	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 2.4mA$	0.26	0.33	0.40	V
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.40	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.40	V
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	4	40	160	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency, (50% duty cycle)	f_{max}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	10	10	10	ns
		3.0V		20	20	20	
		4.5V		40	35	30	
		6.0V		50	45	40	
Maximum Propagation Delay, CLK to Q	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, $t_r = t_f = 6ns$	160	200	250	ns
		3.0V		100	150	200	
		4.5V		32	40	48	
		6.0V		27	34	42	

5. Not production tested in die form, characterized by chip design and tested in package.

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, CLR to Q	t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	175	220	265	ns
		3.0V		100	150	200	
		4.5V		35	44	53	
		6.0V		30	37	45	
Maximum Output Transition time, Any Output	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	110	ns
		3.0V		27	32	36	
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[6]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				180			

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, A or B to Clock	t_{su}	2.0V	$t_r = t_f$ = 6ns	25	35	40	ns
		3.0V		15	20	25	
		4.5V		7	8	9	
		6.0V		5	6	6	
Minimum Hold Time, Clocl to A or B	t_h	2.0V	$t_r = t_f$ = 6ns	3	3	3	ns
		3.0V		3	3	3	
		4.5V		3	3	3	
		6.0V		3	3	3	
Minimum Recovery Time, Reset Inactive to Clock	t_{rec}	2.0V	$t_r = t_f$ = 6ns	3	3	3	ns
		3.0V		3	3	3	
		4.5V		3	3	3	
		6.0V		3	3	3	
Minimum Pulse Width, Clock	t_w	2.0V	$t_r = t_f$ = 6ns	50	60	75	ns
		3.0V		26	35	45	
		4.5V		12	15	20	
		6.0V		10	12	15	
Maximum Input Rise & Fall Times	t_r, t_f	2.0V	$t_r = t_f$ = 6ns	1000	1000	1000	ns
		3.0V		800	800	800	
		4.5V		500	500	500	
		6.0V		400	400	400	

Switching Waveforms

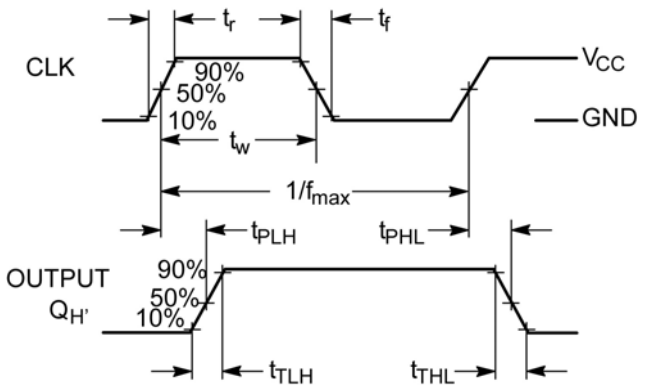


Figure 1 – Clock Propagation Delay & Output Timing

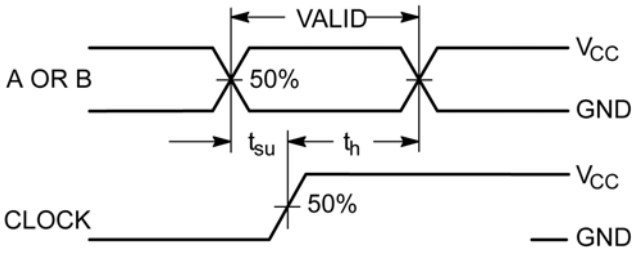


Figure 2 – Data Transition Timing, Serial Input & Clock

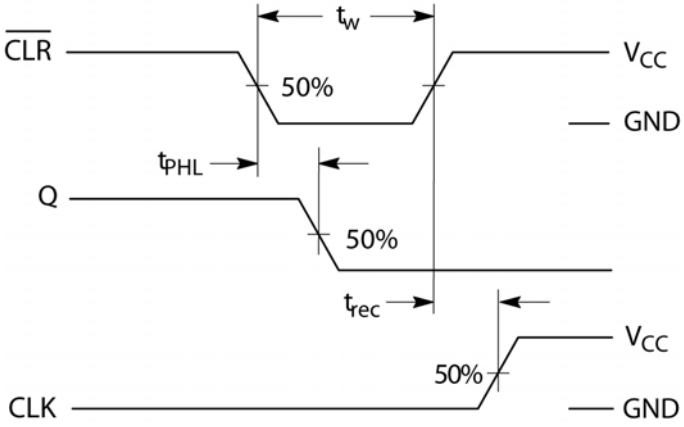
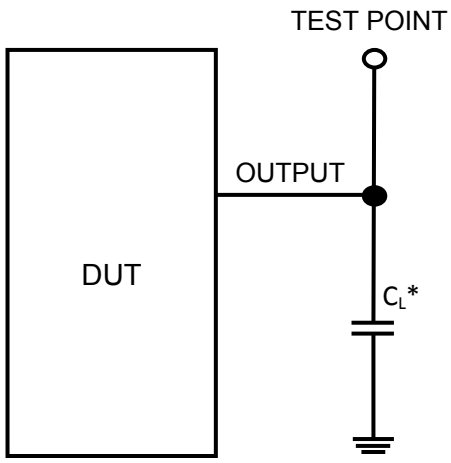


Figure 3 – Reset to Output Propagation Delay & Timing



* Includes all probe and jig capacitance

Figure 4 – Test Setup