# High Speed CMOS Logic – 54HC154

**Dual 1-of-16 Decoder / Demultiplexer in bare die form**

**Rev 1.0**
**30/05/22**

## Description

The 54HC154 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. The device consists of x4 active-high binary address inputs, x16 active-low outputs & x2 active-low chip-selects. The x2 active-low chip-selects can be used to strobe & eliminate normal decoding 'glitches' on the outputs, or can be used to expand the decoder. Both chip-selects must be low to enable the outputs. The demultiplexing function is executed by use of one chip-select input as multiplexed data input. When the other chip-select input is low, the addressed output will follow the state of the applied data.

## Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS154
- Full Military Temperature Range.

## Ordering Information

The following part suffixes apply:

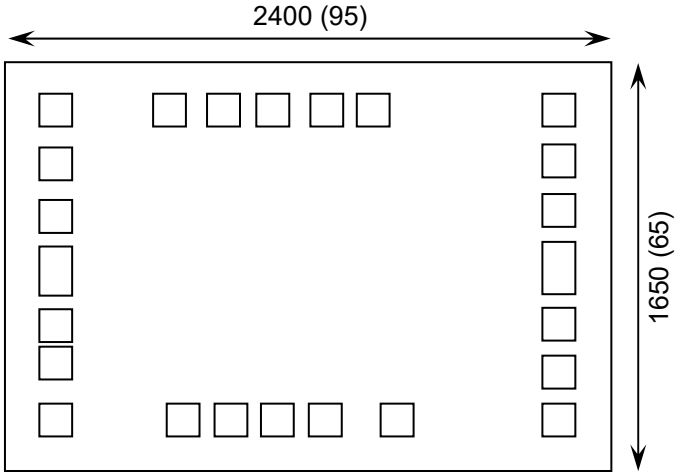
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

## Die Dimensions in µm (mils)




## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

| | | |
|---|---|---|
| Die Size (Unsawn) | 2400 x 1650<br>95 x 65 | µm<br>mils |
| Minimum Bond Pad Size | 120 x 120<br>4.72 x 4.72 | µm<br>mils |
| Die Thickness | 350 (±20)<br>13.78 (±0.79) | µm<br>mils |
| Top Metal Composition | Al 1%Si 1.1µm | |
| Back Metal Composition | N/A – Bare Si | |

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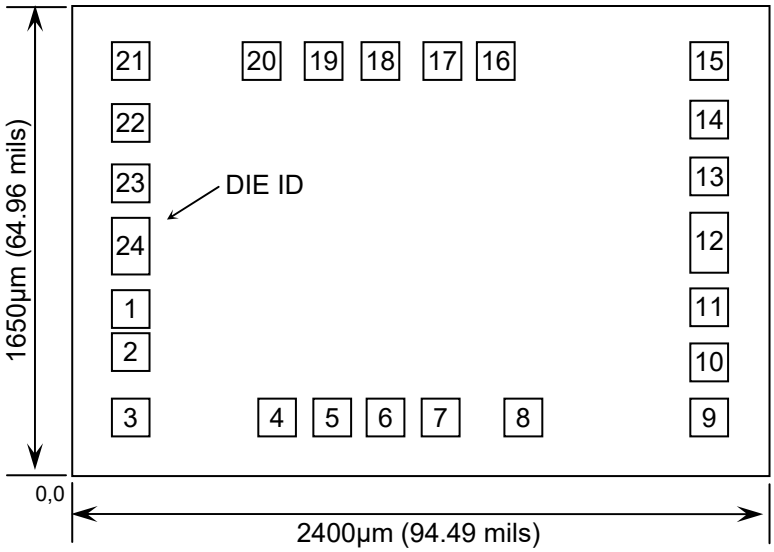
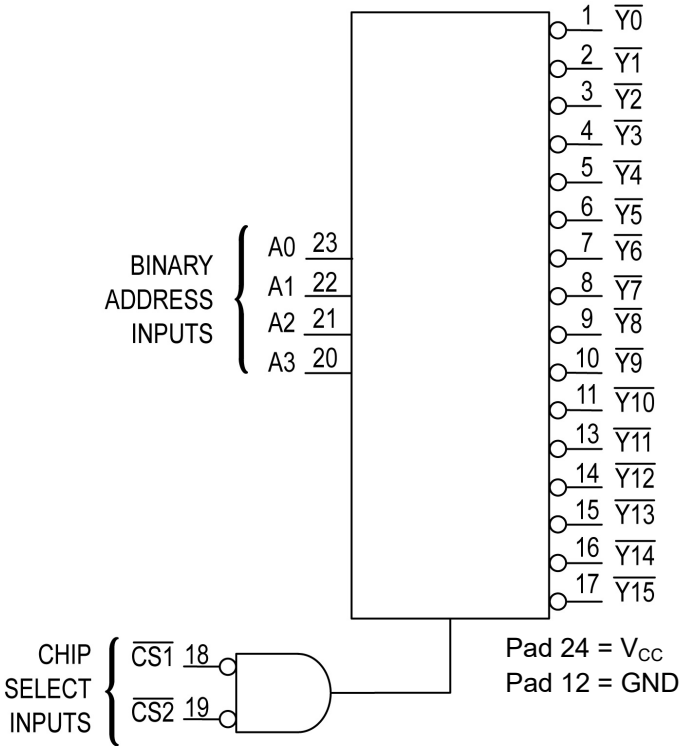
## Pad Layout and Functions




| PAD | FUNCTION | COORDINATES (mm) | |
|---|---|---|---|
| | | X | Y |
| 1 | $\overline{Y0}$ | 0.140 | 0.522 |
| 2 | $\overline{Y1}$ | 0.140 | 0.377 |
| 3 | $\overline{Y2}$ | 0.140 | 0.142 |
| 4 | $\overline{Y3}$ | 0.645 | 0.132 |
| 5 | $\overline{Y4}$ | 0.833 | 0.132 |
| 6 | $\overline{Y5}$ | 1.021 | 0.132 |
| 7 | $\overline{Y6}$ | 1.210 | 0.132 |
| 8 | $\overline{Y7}$ | 1.490 | 0.132 |
| 9 | $\overline{Y8}$ | 2.138 | 0.142 |
| 10 | $\overline{Y9}$ | 2.138 | 0.342 |
| 11 | $\overline{Y10}$ | 2.138 | 0.537 |
| 12 | GND | 2.138 | 0.724 |
| 13 | $\overline{Y11}$ | 2.138 | 0.992 |
| 14 | $\overline{Y12}$ | 2.138 | 1.187 |
| 15 | $\overline{Y13}$ | 2.138 | 1.387 |
| 16 | $\overline{Y14}$ | 1.397 | 1.490 |
| 17 | $\overline{Y15}$ | 1.210 | 1.397 |
| 18 | $\overline{CS1}$ | 1.005 | 1.397 |
| 19 | $\overline{CS2}$ | 0.795 | 1.397 |
| 20 | A3 | 0.590 | 1.397 |
| 21 | A2 | 0.140 | 1.387 |
| 22 | A1 | 0.140 | 1.179 |
| 23 | A0 | 0.140 | 0.971 |
| 24 | $V_{CC}$ | 0.140 | 0.707 |
| CONNECT CHIP BACK TO $V_{CC}$ OR FLOAT | | | |

## Logic Diagram




## Truth Table

SEE PAGE 5

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## Absolute Maximum Ratings[1]

| PARAMETER | SYMBOL | VALUE | UNIT |
|---|---|---|---|
| DC Supply Voltage (Referenced to GND) | $V_{CC}$ | -0.5 to +7.0 | V |
| DC Input Voltage (Referenced to GND) | $V_{IN}$ | -1.5 to $V_{CC}$ +1.5 | V |
| DC Output Voltage (Referenced to GND) | $V_{OUT}$ | -0.5 to $V_{CC}$ +0.5 | V |
| DC Input Current, per pin | $I_{IN}$ | ±20 | mA |
| DC Output Current, per pin | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$ or GND Current, per pin | $I_{CC}$ | ±50 | mA |
| Power Dissipation in Still Air[2] | $P_D$ | 750 | mW |
| Storage Temperature Range | $T_{STG}$ | -65 to 150 | °C |

**1.** Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions[3] (Voltages referenced to GND)

| PARAMETER | | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| DC Supply Voltage | | $V_{CC}$ | 2 | 6 | V |
| DC Input or Output Voltage | | $V_{IN}$ ,$V_{OUT}$ | 0 | $V_{CC}$ | V |
| Operating Temperature Range | | $T_J$ | -55 | +125 | °C |
| Input Rise and Fall Time | $V_{CC}$ = 2.0V | $t_r$, $t_f$ | 0 | 1000 | ns |
| | $V_{CC}$ = 4.5V | | 0 | 500 | |
| | $V_{CC}$ = 6.0V | | 0 | 400 | |

**3.** This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range GND ≤ ($V_{IN}$ or $V_{OUT}$) ≤ $V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages Referenced to GND)

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Minimum High-Level Input Voltage | $V_{IH}$ | 2.0V | $V_{OUT}$ = 0.1V or $V_{CC}$ -0.1V<br>$\lvert I_{OUT} \rvert$ ≤ 20μA | 1.5 | 1.5 | 1.5 | V |
| | | 4.5V | | 3.15 | 3.15 | 3.15 | |
| | | 6.0V | | 4.2 | 4.2 | 4.2 | |
| Maximum Low-Level Input Voltage | $V_{IL}$ | 2.0V | $V_{OUT}$ = 0.1V or $V_{CC}$ -0.1V<br>$\lvert I_{OUT} \rvert$ ≤ 20μA | 0.3 | 0.3 | 0.3 | V |
| | | 4.5V | | 0.9 | 0.9 | 0.9 | |
| | | 6.0V | | 1.2 | 1.2 | 1.2 | |

**4.** -55°C ≤ $T_J$ ≤ +125°C

## DC Electrical Characteristics (Voltages Referenced to GND)

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Minimum High-Level Output Voltage | $V_{OH}$ | 2.0V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 20\mu A$ | 1.9 | 1.9 | 1.9 | V |
| | | 4.5V | | 4.4 | 4.4 | 4.4 | |
| | | 6.0V | | 5.9 | 5.9 | 5.9 | |
| | | 4.5V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 4.0mA$ | 3.98 | 3.84 | 3.70 | |
| | | 6.0V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 5.2mA$ | 5.48 | 5.34 | 5.20 | |
| Maximum Low-Level Output Voltage | $V_{OL}$ | 2.0V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 20\mu A$ | 0.1 | 0.1 | 0.1 | V |
| | | 4.5V | | 0.1 | 0.1 | 0.1 | |
| | | 6.0V | | 0.1 | 0.1 | 0.1 | |
| | | 4.5V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 4.0mA$ | 0.26 | 0.33 | 0.40 | |
| | | 6.0V | $V_{IN} = V_{IH}$ or $V_{IL}$ $\lvert I_{OUT} \rvert \leq 5.2mA$ | 0.26 | 0.33 | 0.40 | |
| Maximum Input Leakage Current | $I_{IN}$ | 6.0V | $V_{IN} = V_{CC}$ or GND | ±0.1 | ±1.0 | ±1.0 | µA |
| Maximum Quiescent Supply Current | $I_{CC}$ | 6.0V | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$ | 8 | 80 | 160 | µA |

## AC Electrical Characteristics[5]

| PARAMETER | SYMBOL | $V_{CC}$ | CONDITIONS | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | 25°C | 85°C | FULL RANGE[4] | |
| Maximum Propagation Delay, Select to Output Y (Figure 1, 3) | $t_{PLH}$, $t_{PHL}$ | 2.0V | $C_L = 50pF$, $t_r = t_f = 6ns$ | 190 | 240 | 285 | ns |
| | | 4.5V | | 38 | 48 | 57 | |
| | | 6.0V | | 32 | 41 | 48 | |
| Maximum Propagation Delay, Input A to Output Y (Figure 2,3) | $t_{PLH}$, $t_{PHL}$ | 2.0V | $C_L = 50pF$, $t_r = t_f = 6ns$ | 175 | 220 | 265 | ns |
| | | 4.5V | | 35 | 44 | 53 | |
| | | 6.0V | | 30 | 37 | 45 | |
| Maximum Output Transition Time, Any Output (Figure 1,3) | $t_{TLH}$, $t_{THL}$ | 2.0V | $C_L = 50pF$, $t_r = t_f = 6ns$ | 75 | 95 | 110 | ns |
| | | 4.5V | | 15 | 19 | 22 | |
| | | 6.0V | | 13 | 16 | 19 | |
| Maximum Input Capacitance | $C_{IN}$ | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance[7] | $C_{PD}$ | - | $T_J = 25°C$, $V_{CC} = 5.0V$ | TYPICAL | | | |
| | | | | 80 | | | pF |

**6.** Not production tested in die form, characterized by chip design and tested in package.
**7.** Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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## Pad Description

**ADDRESS INPUTS**
**A0, A1, A2, A3**
**(Pads 23, 22, 21, 20)**
These inputs, when the 1-of-16 decoder is enabled, determine which of its sixteen active-low outputs is selected.

**CONTROL INPUTS**
**$\overline{CS1}$, $\overline{CS2}$**
**(Pads 18, 19)**
Active-low chip-select inputs. With a low level on both inputs, the outputs of the decoder follow the Address inputs. A high level on either input forces all outputs to a high level.

**OUTPUTS**
**Y0, Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15**
**(Pads 1-11, Pads 13-17)**
Active-low outputs. These outputs assume a low level when addressed and both chip-select inputs are active. These outputs remain high when not addressed or when a chip-select input is high.

## Truth Table

| INPUTS | | | | | | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CS1 | CS2 | A3 | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 | Y10 | Y11 | Y12 | Y13 | Y14 | Y15 |
| L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | L | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | L | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H | H |
| L | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H | H |
| L | L | H | H | L | L | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| L | L | H | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | L |
| L | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | L | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |
| H | H | X | X | X | X | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H | H |

H = High Level, L = Low Level, X = Don't Care

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## Switching Waveforms

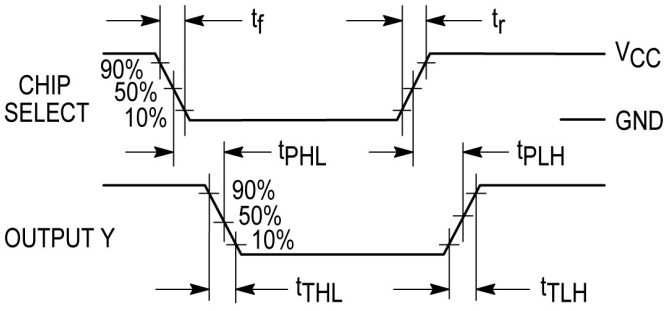



**Figure 1**

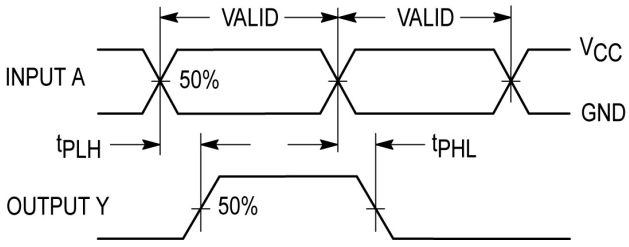
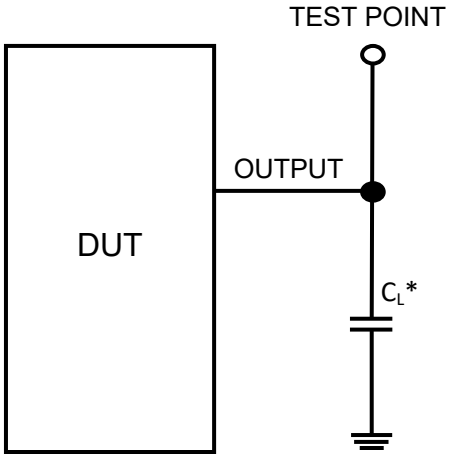



**Figure 2**

## Test Circuit




* Includes all probe and jig capacitance

**Figure 3**