High Speed CMOS Logic – 54HC138

3-Line to 8-Line Decoder / Demultiplexer in bare die form

Rev 1.0
23/11/17

Description

The 54HC138 is fabricated using a 2.5µm 5V CMOS process with the same high speed performance of LSTTL combined with CMOS low power consumption. Inputs are compatible with standard CMOS outputs and LSTTL outputs by using pull-up resistors. The device decodes a three–bit Address to one–of–eight active–low outputs. Featuring three Chip Select inputs, two active–low & one active–high to facilitate the demultiplexing, cascading, and chip–selecting functions. The demultiplexing function uses the Address inputs to select desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS138
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

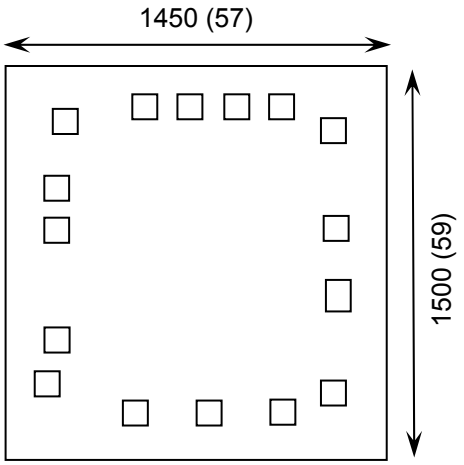
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For more information on LAT flows please see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1450 x 1500 57 x 59	µm mils
Minimum Bond Pad Size	100 x 100 4 x 4	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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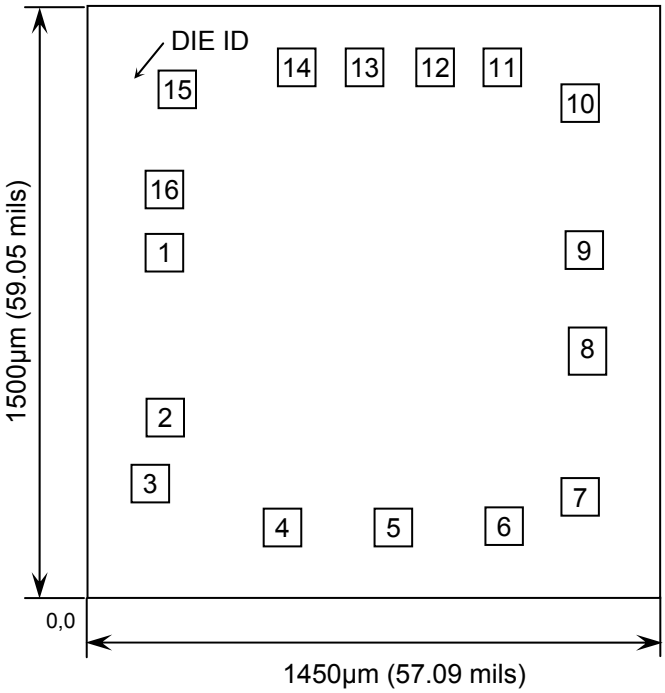
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A0	0.149	0.823
2	A1	0.149	0.409
3	A2	0.111	0.239
4	CS2	0.446	0.129
5	CS3	0.723	0.129
6	CS1	1.004	0.129
7	Y7	1.195	0.203
8	GND	1.217	0.566
9	Y6	1.207	0.832
10	Y5	1.197	1.204
11	Y4	1.000	1.294
12	Y3	0.827	1.294
13	Y2	0.653	1.294
14	Y1	0.479	1.294
15	Y0	0.178	1.238
16	V_{CC}	0.147	0.980
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Truth Table

INPUTS						OUTPUTS							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High level (steady state)
L = Low level (steady state)
X = Don't care

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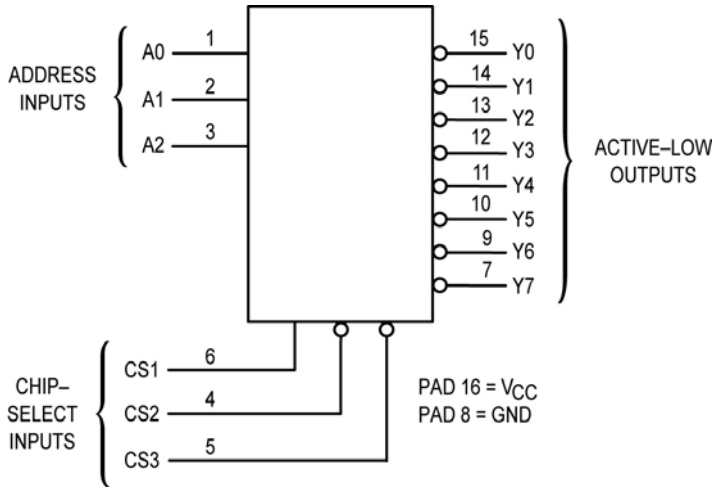
Logic Diagram



Pad Descriptions

ADDRESS INPUTS
A0, A1, A2 (Pads 1, 2, 3)
Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active–low.

CONTROL INPUTS
CS1, CS2, CS3 (Pads 6, 4, 5)
Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

OUTPUTS
Y0 – Y7 (Pads 15, 14, 13, 12, 11, 10, 9, 7)
Active–low Decoded outputs. These outputs assume a low level when addressed and the chip is selected. These outputs remain high when not addressed or the chip is not selected.

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Input Rise and Fall Times (Figure 2)	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[3]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \leq 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\| \leq 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 2.4mA$	2.48	2.34	2.2	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0mA$	3.98	3.84	3.70	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 5.2mA$	5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 2.4mA$	0.26	0.33	0.40	V
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0mA$	0.26	0.33	0.40	
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 5.2mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	4	40	160	µA

3. -55°C ≤ T_J ≤ +125°C

AC Electrical Characteristics[4]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[3]	
Maximum Propagation Delay, Input A to Output Y (Figure 1, 4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	135	170	205	ns
		3.0V		90	125	165	
		4.5V		27	34	41	
		6.0V		23	29	35	
Maximum Propagation Delay, CS1 to Output Y (Figure 2, 4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	110	140	165	ns
		3.0V		85	100	125	
		4.5V		22	28	33	
		6.0V		19	24	28	
Maximum Propagation Delay, CS2 or CS3 to Output Y (Figure 3, 4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	120	150	180	ns
		3.0		90	120	150	
		4.5V		24	30	36	
		6.0V		20	26	31	
Maximum Output Rise and Fall Time, Any Output (Figure 2, 4)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	110	ns
		3.0V		30	40	55	
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance[5]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				55			

4. Not production tested in die form, characterized by chip design and tested in package.
5. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveforms

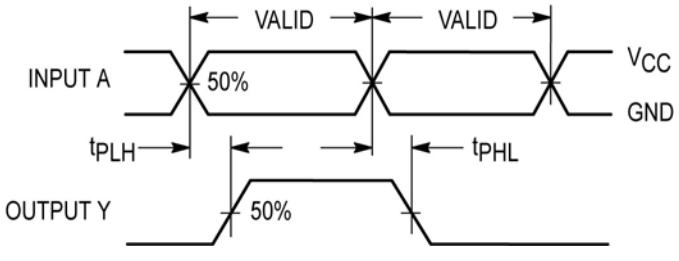


Figure 1 – Propagation Delay, Input A to Output Y

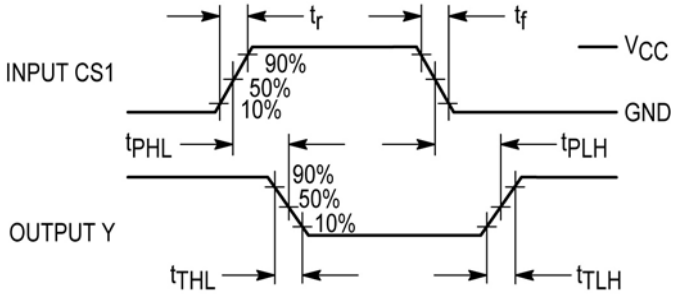


Figure 2 - Propagation Delay, Input CS1 to Output Y

Switching Waveforms

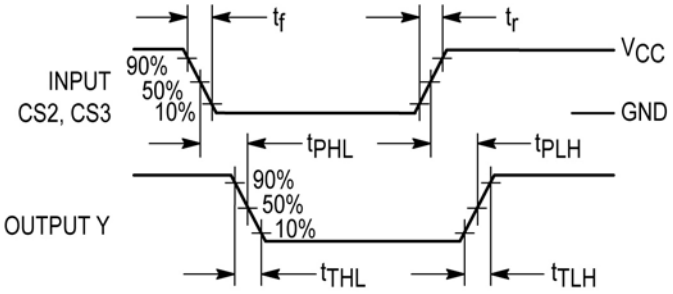
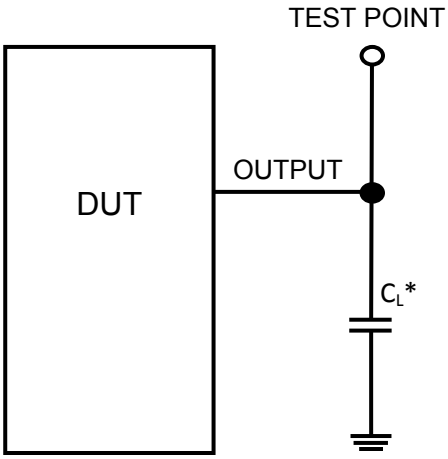


Figure 3 – Propagation Delay, Input CS2 to Output Y

Test Circuit



* Includes all probe and jig capacitance

Figure 4