



High Speed CMOS Logic – 54HC132

Quadruple 2-Input NAND Gate IC with Schmitt-Trigger Inputs in bare die form

Rev 1.0
21/11/17

Description

The 54HC132 is fabricated using a 2.5 μ m 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. The hysteresis characteristics (around 20% V_{CC}) of all inputs allow slowly changing input signals to be transformed into sharply defined jitter-free output signals. All inputs are compatible with standard CMOS outputs; using pull-up resistors, they are compatible with LSTTL outputs. Inputs are also equipped with protection circuits against static discharge and transient excess voltage.

Ordering Information

The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection
- “H” - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- “K” - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

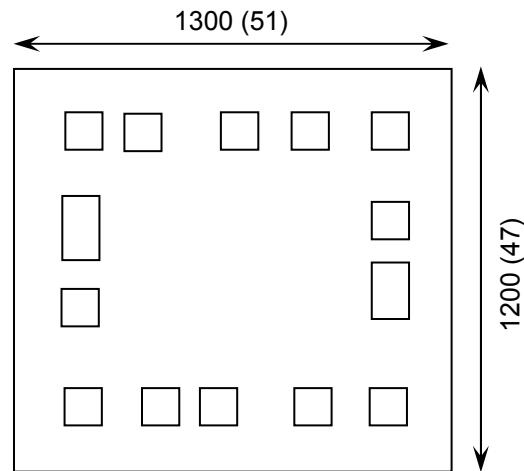
Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350 μ m(14 Mils) – On request
- Assembled into Ceramic Package – On request

Features:

- High Speed: t_{PD} = 11ns @ 5V (Typ.)
- Low Input Current: 1 μ A
- Output Drive Capability: 10 LSTTL loads
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS132
- Full Military Temperature Range.

Die Dimensions in μ m (mils)



Mechanical Specification

Die Size (Unsawn)	1300 x 1200 51 x 47	μ m mils
Minimum Bond Pad Size	106 x 106 4 x 4	μ m mils
Die Thickness	350 (\pm 20) 13.78 (\pm 0.79)	μ m mils
Top Metal Composition	Al 1%Si 1.1 μ m	
Back Metal Composition	N/A – Bare Si	



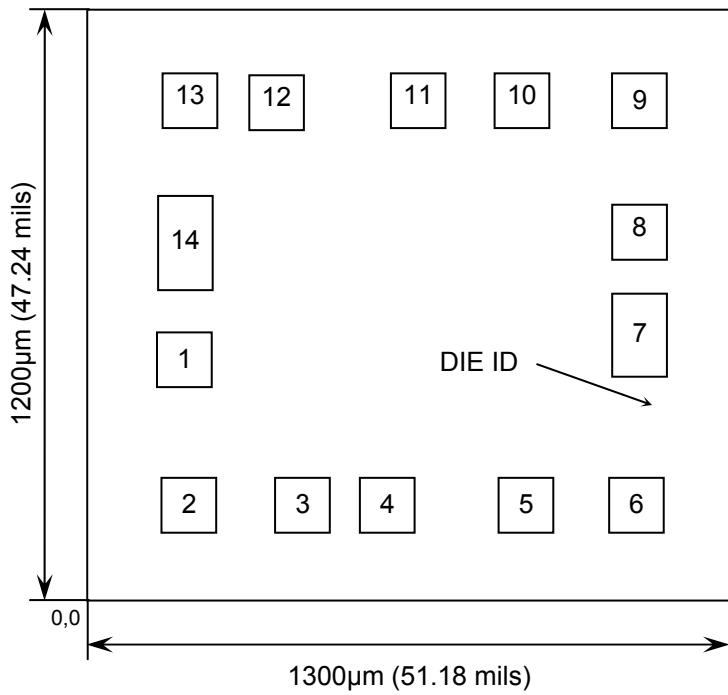


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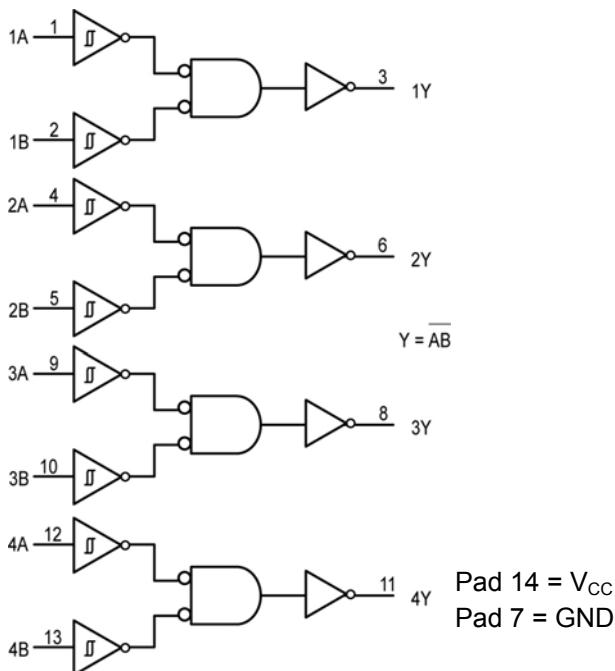
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.143	0.434
2	1B	0.153	0.14
3	1Y	0.383	0.14
4	2A	0.551	0.14
5	2B	0.834	0.14
6	2Y	1.062	0.14
7	GND	1.064	0.458
8	3Y	1.064	0.697
9	3A	1.064	0.96
10	3B	0.826	0.96
11	4Y	0.619	0.96
12	4A	0.333	0.96
13	4B	0.143	0.96
14	V _{CC}	0.143	0.634

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram



Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High level (steady state)

L = Low level (steady state)





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-1.5 to V _{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
Clamp Diode Current	I _{IK} , I _{OK}	±20	mA
DC Output Current, per pad	I _{OUT}	±25	mA
DC V _{CC} or GND Current, per pad	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V _{CC}	2	6	V
DC Input or Output Voltage	V _{IN} , V _{OUT}	0	V _{CC}	V
Operating Temperature Range	T _J	-55	+125	°C
Input Rise or Fall Times	t _r , t _f	V _{CC} = 2.0V	-	No limit*

* When V_{IN} ~ 0.5 V_{CC}, I_{CC} >> quiescent current.

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Positive-Going Input Threshold Voltage	V _{T+} MAX	2V	V _{OUT} = 0.1V I _{OUT} ≤ 20µA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Minimum Positive-Going Input Threshold Voltage	V _{T+} MIN	2V	V _{OUT} = 0.1V I _{OUT} ≤ 20µA	1.0	0.95	0.95	V
		4.5V		2.3	2.25	2.25	
		6.0V		3.0	2.95	2.95	
Maximum Negative-Going Input Threshold Voltage	V _{T-} MAX	2V	V _{OUT} = V _{CC} -0.1V I _{OUT} ≤ 20µA	0.9	0.95	0.95	V
		4.5V		2.0	2.05	2.05	
		6.0V		2.6	2.65	2.65	
Minimum Negative-Going Input Threshold Voltage	V _{T-} MIN	2V	V _{OUT} = V _{CC} -0.1V I _{OUT} ≤ 20µA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	





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DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Hysteresis Voltage ⁵	V _{H MAX}	2V	V _{OUT} = 0.1V or V _{CC} - 0.1V I _{OUT} ≤ 20µA	1.2	1.2	1.2	V
		4.5V		2.25	2.25	2.25	
		6.0V		3.0	3.0	3.0	
Minimum Hysteresis Voltage	V _{H MIN}	2V	V _{OUT} = 0.1V or V _{CC} - 0.1V I _{OUT} ≤ 20µA	0.2	0.2	0.2	V
		4.5V		0.4	0.4	0.4	
		6.0V		0.5	0.5	0.5	
Minimum High-Level Output Voltage	V _{OH}	2V	V _{IN} ≤ V _{T- MIN} or V _{T+ MAX} I _{OUT} ≤ 20µA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	V _{IN} ≤ V _{T- MIN} or V _{T+ MAX} I _{OUT} ≤ 4.0mA	3.98	3.84	3.7	V
		6.0V	V _{IN} ≤ V _{T- MIN} or V _{T+ MAX} I _{OUT} ≤ 5.2mA	5.48	5.34	5.2	
		2V	V _{IN} ≥ V _{T+ MAX} I _{OUT} ≤ 20µA	0.1	0.1	0.1	V
Maximum Low-Level Output Voltage	V _{OL}	4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	V _{IN} ≥ V _{T+ MAX} I _{OUT} ≤ 4.0mA	0.26	0.33	0.4	V
		6.0V	V _{IN} ≥ V _{T+ MAX} I _{OUT} ≤ 5.2mA	0.26	0.33	0.4	
Maximum Input Leakage Current	I _{IN}	6.0V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I _{CC}	6.0V	V _{IN} = V _{CC} or GND, I _{OUT} = 0µA	1.0	10	40	µA

4. -55°C ≤ T_J ≤ +125°C

5. V_{H MIN} > (V_{T+ MIN}) - (V_{T- MAX}); V_{H MAX} = (V_{T+ MAX}) + (V_{T- MIN})





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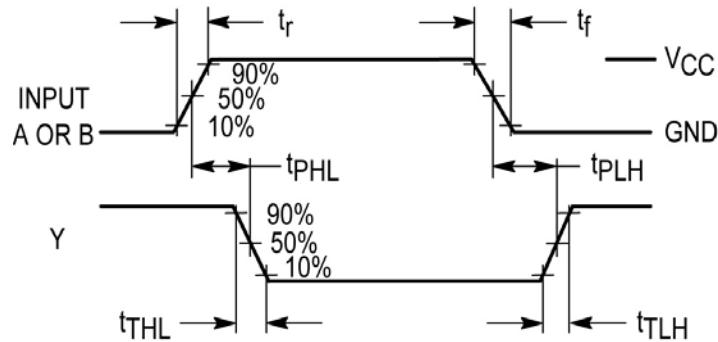
AC Electrical Characteristics⁶

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Propagation Delay, Input A or B to Output Y	t _{PLH} , t _{PHL}	2V	C _L = 50pF, t _r = t _f = 6ns	125	155	190	ns
		4.5V		25	31	38	
		6.0V		21	26	32	
Maximum Output Rise and Fall Time, Any Output	t _{TLH} , t _{THL}	2V	C _L = 50pF, t _r = t _f = 6ns	75	95	110	ns
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate ⁷	C _{PD}	-	T _A = 25°C, V _{CC} = 5.0V	TYPICAL			pF
				24			

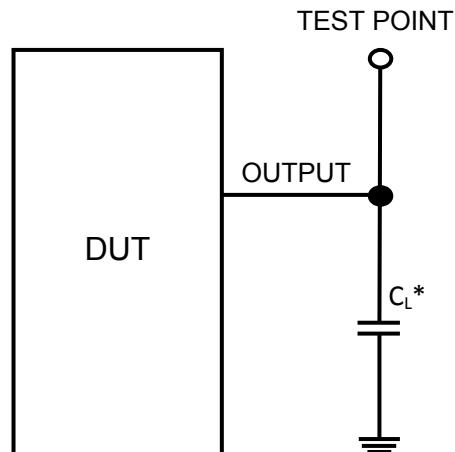
6. Not production tested in die form, characterized by chip design and tested in package.

7. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}.

Switching Waveform



Test Circuit



* Includes all probe and jig capacitance

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