



# High Speed CMOS Logic – 54HC112

Dual J-K Flip-Flops with preset and clear; negative edge trigger in bare die form

Rev 1.0  
24/11/17

## Description

The 54HC112 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. Each flip-flop has independent J, K, preset, clear, clock inputs and Q Q̄ outputs. A high level at the clock input enables the J and K inputs to accept data. The device changes state on the negative going transition of the clock pulse. Preset and clear are independent of the clock and are accomplished by a low logic level on the corresponding input. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## Features:

- Output Drive Capability: 10 LSTTL Loads
- Bus Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 54LS112
- Full Military Temperature Range.

## Ordering Information

The following part suffixes apply:

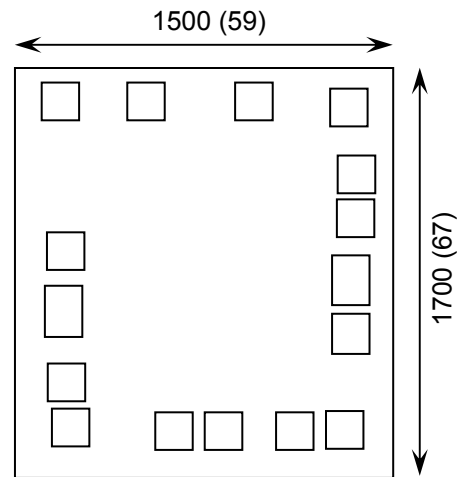
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1500 x 1700 59 x 67	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

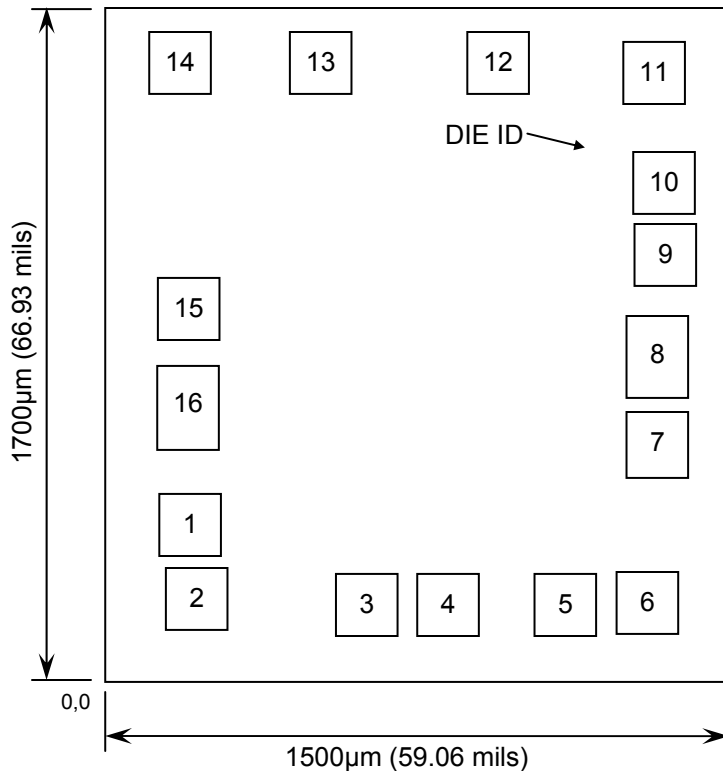




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## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1CLK	0.125	0.345
2	1K	0.135	0.125
3	1J	0.585	0.135
4	1PRE	0.755	0.135
5	1Q	1.025	0.135
6	1Q̄	1.225	0.135
7	2Q̄	1.245	0.54
8	GND	1.245	0.735
9	2Q	1.26	0.995
10	2PRE	1.26	1.165
11	2J	1.25	1.47
12	2K	0.86	1.48
13	2CLK	0.48	1.48
14	2CLR	0.125	1.47
15	1CLR	0.125	0.855
16	V <sub>CC</sub>	0.125	0.615

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

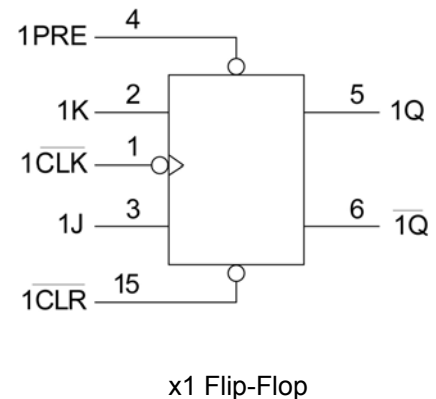
## Truth Table

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	NO CHANGE	

H = High level (steady state), L = Low level (steady state)  
X = Don't care, ↓ = High-to-Low transition

\* Output states unpredictable if both PRE and CLR go High simultaneously after both being low at the same time.

## Logic Diagram





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## Pad Descriptions

### CLOCK INPUTS

**1CLK, 2CLK (Pads 1, 13)**

Clock input (HIGH-to-LOW, edge triggered)

### DATA INPUTS

**1K, 2K, 1J, 2J (Pads 2, 12, 3, 11)**

Data inputs; flip-flops 1 and 2

### OUTPUTS

**1Q, 2Q, 1Q, 2Q (Pads 5, 9, 6, 7)**

True flip-flop outputs and complement flip-flop outputs

### CONTROL INPUTS

**1PRE, 2PRE (Pads 4, 10)**

Set inputs (active LOW)

**1CLR, 2CLR ( Pads 15, 14)**

Reset inputs (active LOW)

### GROUND & POWER

**GND, V<sub>CC</sub> (Pads 8, 16)**

Ground 0V, Positive Supply Voltage

## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	-1.5 to V <sub>CC</sub> +1.5	V
DC Output Voltage (Referenced to GND)	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
DC Input Current, per pin	I <sub>IN</sub>	±20	mA
DC Output Current, per pin	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> or GND Current, per pin	I <sub>CC</sub>	±50	mA
Power Dissipation in Still Air <sup>2</sup>	P <sub>D</sub>	750	mW
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	V <sub>CC</sub>	2	6	V	
DC Input or Output Voltage	V <sub>IN</sub> , V <sub>OUT</sub>	0	V <sub>CC</sub>	V	
Operating Temperature Range	T <sub>J</sub>	-55	+125	°C	
Input Rise and Fall Time	V <sub>CC</sub> = 2.0V	t <sub>r</sub> , t <sub>f</sub>	0	1000	ns
	V <sub>CC</sub> = 4.5V		0	500	
	V <sub>CC</sub> = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>IN</sub> and V<sub>OUT</sub> should be constrained to the range GND ≤ (V<sub>IN</sub> or V<sub>OUT</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.





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## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	V <sub>IH</sub>	2.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V <sub>IL</sub>	2.0V	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V  I <sub>OUT</sub>   ≤ 20μA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	
Minimum High-Level Output Voltage	V <sub>OH</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
	4.5V	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 4.0mA	3.98	3.84	3.70		
	6.0V	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 5.2mA	5.48	5.34	5.20		
Maximum Low-Level Output Voltage	V <sub>OL</sub>	2.0V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
	4.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 4.0mA	0.26	0.33	0.40		
	6.0V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 5.2mA	0.26	0.33	0.40		
Maximum Input Leakage Current	I <sub>IN</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0μA	4	40	80	μA

## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Max Clock Frequency, 50% Duty Cycle (Figure 1, 4)	f <sub>max</sub>	2.0V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	6.0	4.8	4.0	MHz
		4.5V		30	24	20	
		6.0V		35	28	24	
Maximum Propagation Delay, Clock to Q or Q̄ (Figure 1, 4)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	125	155	190	ns
		4.5V		25	31	38	
		6.0V		21	36	32	
Maximum Propagation Delay, Reset to Q or Q̄ (Figure 2,4)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	155	195	235	ns
		4.5V		31	39	47	
		6.0V		26	33	40	





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## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Set to Q or $\bar{Q}$ (Figure 2,4)	$t_{PLH}, t_{PHL}$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	165	205	250	ns
		4.5V		33	41	50	
		6.0V		28	35	43	
Maximum Output Transition time, Any output (Figure 1,4)	$t_{TLH}, t_{THL}$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	75	95	110	ns
		4.5V		15	19	22	
		6.0V		13	16	19	
Maximum Input Capacitance	$C_{IN}$	-	-	10	10	10	pF
Power Dissipation Capacitance <sup>6</sup> (Per Flip-Flop)	$C_{PD}$	-	-	TYPICAL			pF
				35			

## Timing Requirements<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Setup Time, J or K to Clock (Figure 3)	$t_{SU}$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	100	125	150	ns
		4.5V		20	25	30	
		6.0V		17	21	26	
Minimum Hold Time, Clock to J or K (Figure 3)	$t_H$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	3	3	3	ns
		4.5V		3	3	3	
		6.0V		3	3	3	
Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	$t_{rec}$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	100	125	150	ns
		4.5V		20	25	30	
		6.0V		17	21	26	
Minimum Pulse Width, Clock (Figure 1)	$t_w$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	80	100	120	ns
		4.5V		16	20	24	
		6.0V		14	17	20	
Minimum Pulse Width, Set or Reset (Figure 2)	$t_w$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	80	100	120	ns
		4.5V		16	20	24	
		6.0V		14	17	20	
Maximum Input Rise and Fall times (Figure 1)	$t_r, t_f$	2.0V	$C_L = 50\text{pF}, t_r = t_f = 6\text{ns}$	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	

4.  $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

5. Not production tested in die form, characterized by chip design and tested in package.

6. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .





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## Switching Waveforms

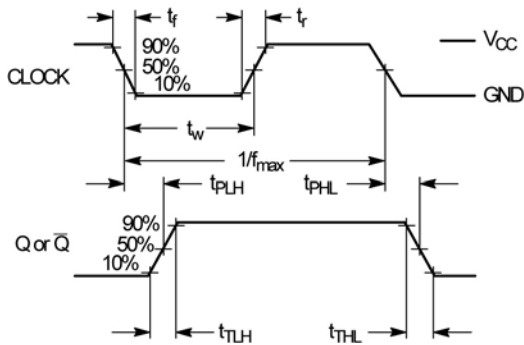


Figure 1 – Propagation Delay & Output transition

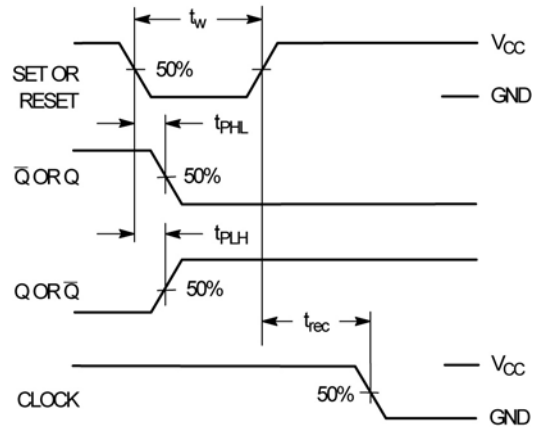


Figure 2 – Propagation Delay, Pulse Width & Recovery

## Test Circuits

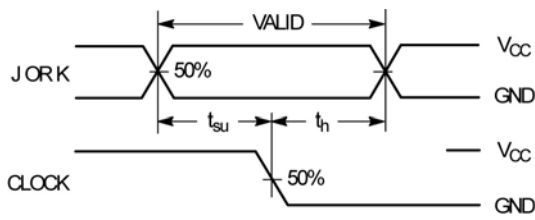
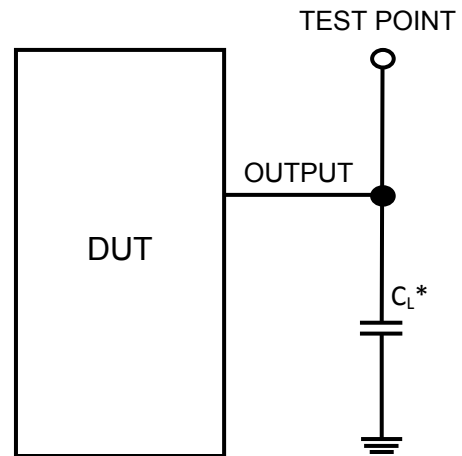


Figure 3 – Setup & Hold time



\* Includes all probe and jig capacitance

Figure 4

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