Advanced Low Power Schottky Logic – 54ALS93

4-bit Binary Counter Logic IC in bare die form

Rev 1.1
28/08/21

Description

The 54ALS93 4-bit binary counter is fabricated using a 2µm 40V bipolar process. The device comprises two 4-bit ripple type counters consisting of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has independent clock (CK) & asynchronous master reset (R0) inputs. Counter state change is triggered by a high-to-low transition on the clock. Each section can be used separately or tied together (Q to CK) to form BCD or modulo-16 counters.

Features:

- Low Power Consumption
- Input Clamp Diodes Limit High Speed Termination Effects
- Full Military Temperature Range.
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

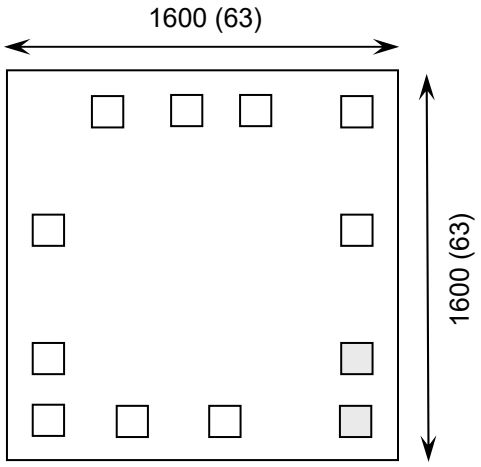
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1600 x 1600 63 x 63	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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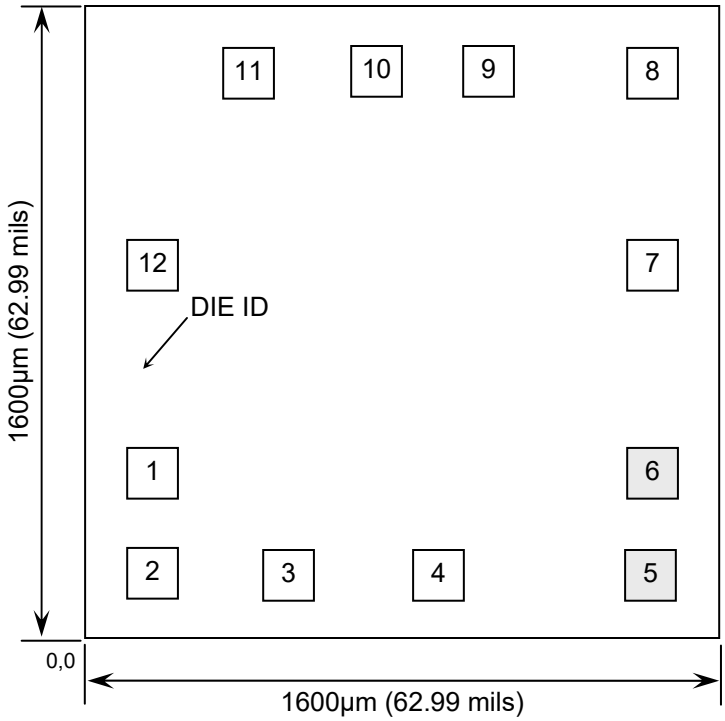
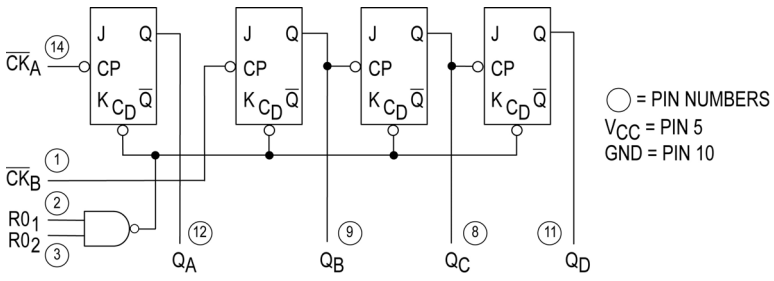
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	CK_B	0.100	0.360
2	$R0_{(1)}$	0.100	0.100
3	$R0_{(2)}$	0.450	0.100
4	V_{CC}	0.830	0.100
5	NC	1.370	0.100
6	NC	1.370	0.360
7	Q_C	1.370	0.880
8	Q_B	1.370	1.370
9	GND	0.960	1.370
10	Q_D	0.670	1.370
11	Q_A	0.350	1.370
12	CK_A	0.100	0.880
CONNECT CHIP BACK TO GND			

Logic Diagram



Truth Table

COUNT	OUTPUT			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: OUTPUT Q_A IS CONNECTED TO INPUT CK_B

H = HIGH Voltage Level
L = LOW Voltage Level

Mode Selection

RESET INPUT		OUTPUT			
$R0_{(1)}$	$R0_{(2)}$	Q_A	Q_B	Q_C	Q_D
H	H	L	L	L	L
L	H	COUNT			
H	L	COUNT			
L	L	COUNT			

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage (Referenced to GND)	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	8	mA
Operating Temperature Range	T_J	-55	+125	°C

DC Electrical Characteristics

Voltages referenced to GND, T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-	2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage	V_{IK}	V_{CC} = 4.5V I_{IN} = -18mA	-	-0.65	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = 4.5V, I_{OH} = -0.4mA	V_{CC} -2	-	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V, I_{OL} = 4mA	-	0.25	0.4	V
		V_{CC} = 4.5V, I_{OL} = 8mA	-	0.35	0.5	
Input High Current	I_{IH}	V_{CC} = 5.5V, V_{IN} = 2.7V	-	-	20	µA
		V_{CC} = 5.5V, V_{IN} = 7.0V	-	-	0.1	mA
Input Low Current	I_{IL}	V_{CC} = 5.5V, V_{IL} = 0.4V	-	-	-0.1	mA
Short Circuit Current[2]	I_{OS}	V_{CC} = 5.5V, V_{OUT} = 2.25V	-30	-	-112	mA
Supply Current	I_{CC}	V_{CC} = 5.5V	-	-	13	mA

2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC Electrical Characteristics[4] V_{CC} = 5V, T_J = -55°C to 125°C unless otherwise specified

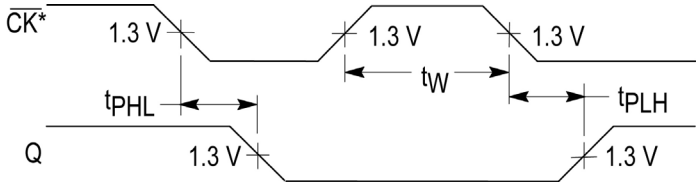
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Clock Frequency, CK_A	f_{max}	C_L = 50pF, R_L = 510Ω	32	-	-	MHz
Input Clock Frequency, CK_B			16	-	-	MHz
Fall, Rising Edge	t_f, t_r		-	-	2	ns
Propagation Delay, CK_A to Q_A	t_{PLH}	C_L = 50pF, R_L = 510Ω	-	-	16	ns
Propagation Delay, CK_A to Q_A	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	18	
Propagation Delay, CK_A to Q_D	t_{PLH}	C_L = 50pF, R_L = 510Ω	-	-	70	ns
Propagation Delay, CK_A to Q_D	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	70	ns
Propagation Delay, CK_B to Q_B	t_{PLH}	C_L = 50pF, R_L = 510Ω	-	-	16	ns
Propagation Delay, CK_B to Q_B	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	21	ns
Propagation Delay, CK_B to Q_C	t_{PLH}	C_L = 50pF, R_L = 510Ω	-	-	32	ns
Propagation Delay, CK_B to Q_C	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	35	ns
Propagation Delay, CK_B to Q_D	t_{PLH}	C_L = 50pF, R_L = 510Ω	-	-	51	ns
Propagation Delay, CK_B to Q_D	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	51	ns
Propagation Delay, R0 to any output	t_{PHL}	C_L = 50pF, R_L = 510Ω	-	-	32	ns

Timing Requirements[4] V_{CC} = 5V, T_J = -55°C to 125°C unless otherwise specified

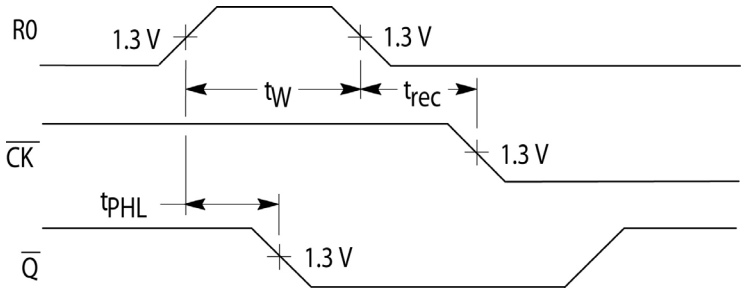
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
CK_A Pulse Width	t_W	C_L = 50pF, R_L = 510Ω	15	-	-	ns
CK_B Pulse Width			30	-	-	ns
R0 Pulse Width			15	-	-	ns
Recovery Time, R0 to CK	t_{REC}	C_L = 50pF, R_L = 510Ω	25	-	-	ns

4. Not production tested in die form, characterized by chip design.

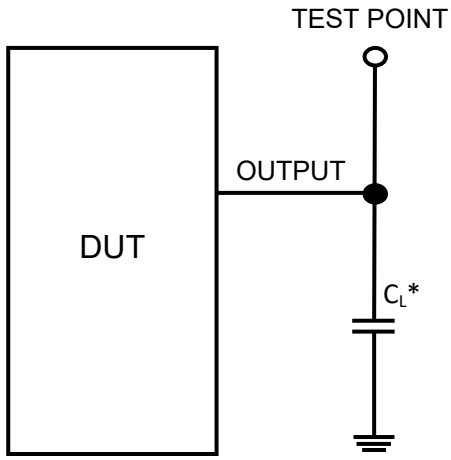
Switching Waveforms



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table.



Test Circuit



* Includes all probe and jig capacitance

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