Advanced Low Power Schottky Logic – 54ALS93

#### 4-bit Binary Counter Logic IC in bare die form

### Description

The 54ALS93 4-bit binary counter is fabricated using a 2µm 40V bipolar process. The device comprises two 4-bit ripple type counters consisting of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has independent clock (CK) & asynchronous master reset (R0) inputs. Counter state change is triggered by a high-to-low transition on the clock. Each section can be used separately or tied together (Q to CK) to form BCD or modulo-16 counters.

#### Features:

- Low Power Consumption
- Input Clamp Diodes Limit High Speed Termination Effects
- Full Military Temperature Range.
- Direct drop-in replacement for obsolete components in long term programs.

#### **Ordering Information**

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

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LAT = Lot Acceptance Test.
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For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

### Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

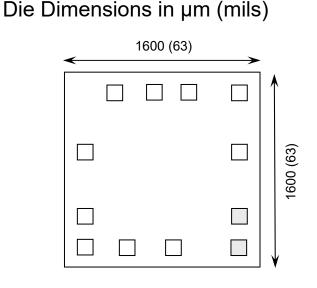
# Mechanical Specification

Die Size (Unsawn)	1600 x 1600 63 x 63	µm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1µm		
Back Metal Composition	N/A – Bare Si		



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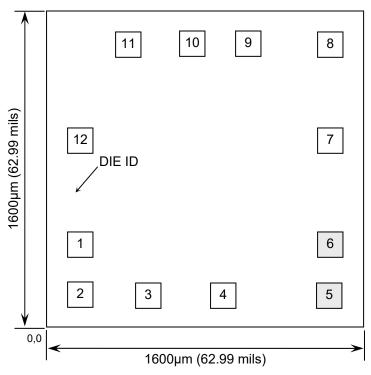
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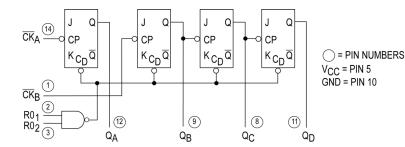
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### Pad Layout and Functions



PAD FUNCTION	FUNCTION	COORDINA	ATES (mm)
	TONOTION	X	Y
1	CK <sub>B</sub>	0.100	0.360
2	R0 <sub>(1)</sub>	0.100	0.100
3	R0 <sub>(2)</sub>	0.450	0.100
4	V <sub>CC</sub>	0.830	0.100
5	NC	1.370	0.100
6	NC	1.370	0.360
7	Q <sub>c</sub>	1.370	0.880
8	Q <sub>B</sub>	1.370	1.370
9	GND	0.960	1.370
10	Q <sub>D</sub>	0.670	1.370
11	Q <sub>A</sub>	0.350	1.370
12	CK <sub>A</sub>	0.100	0.880
	CONNECT CHI	P BACK TO	GND

### Logic Diagram



### Mode Selection

RESET	RESET INPUT		OUTPUT			
R0 <sub>(1)</sub>	R0 <sub>(2)</sub>	Q <sub>A</sub>	$Q_B$	$Q_C$	$Q_D$	
Н	Н	L	L	L	L	
L	Н	COUNT				
Н	L	COUNT				
L	L	COUNT				

### Truth Table

COUNT		OUT	PUT			
000111	Q <sub>A</sub>	Q <sub>B</sub>	$Q_C$	$Q_D$		
0	L	L	L	L		
1	H	L	L	L		
2	L	Н	L L	L		
3	H	Н	L	L		
4	L	L	H	L L L		
5	H	L	H	L		
6	L	Н	H			
7	H	Н	H	L		
8	L	L	L	Н		
9	H	L	L	Н		
10	L	Н	L	Н		
11	H	Н	L	Н		
12	L	L	H	Н		
13	H	L	H	Н		
14	L	Н	H	Н		
15	Н	Н	Н	Н		
NOTE: OUTPUT $Q_A$ IS CONNECTED TO INPUT $CK_B$						
H = HIGH Voltage Level L = LOW Voltage Level						





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### Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V <sub>CC</sub>	7.0	V
DC Input Voltage (Referenced to GND)	V <sub>IN</sub>	7.0	V
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	C°

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

#### **Recommended Operating Conditions**

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage (Referenced to GND)	V <sub>CC</sub>	4.5	5.5	V
High-Level Input Voltage	V <sub>IH</sub>	2	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	0.8	V
High-Level Output Current	I <sub>ОН</sub>	-	-0.4	mA
Low-Level Output Current	I <sub>OL</sub>	-	8	mA
Operating Temperature Range	TJ	-55	+125	°C

#### DC Electrical Characteristics Voltages referenced to GND, T<sub>J</sub> = -55°C to 125°C unless otherwise specified

PARAMETER	SAMBOI	SYMBOL CONDITIONS		LIMITS		
PARAWETER	STINBOL CONDITIONS	MIN	ТҮР	MAX	UNITS	
Minimum High-Level Input Voltage	V <sub>IH</sub>	-	2	-	-	V
Maximum Low-Level Input Voltage	V <sub>IL</sub>	-	-	-	0.8	V
Input Clamp Diode Voltage	VIK	V <sub>CC</sub> = 4.5V I <sub>IN</sub> = -18mA	-	-0.65	-1.5	V
Output Voltage High	V <sub>OH</sub>	V <sub>CC</sub> = 4.5V, I <sub>OH</sub> = -0.4mA	V <sub>CC</sub> -2	-	-	V
Output Voltage Low	V <sub>OL</sub>	$V_{CC}$ = 4.5V, $I_{OL}$ = 4mA	-	0.25	0.4	V
	VOL	$V_{CC}$ = 4.5V, $I_{OL}$ = 8mA	-	0.35	0.5	
Input High Current		$V_{CC} = 5.5 V, V_{IN} = 2.7 V$	-	-	20	μA
Input High Current	I <sub>IH</sub>	$V_{CC} = 5.5 V, V_{IN} = 7.0 V$	-	-	0.1	mA
Input Low Current	IIL	$V_{CC} = 5.5 V, V_{IL} = 0.4 V$	-	-	-0.1	mA
Short Circuit Current <sup>2</sup>	I <sub>OS</sub>	$V_{CC}$ = 5.5V, $V_{OUT}$ = 2.25V	-30	-	-112	mA
Supply Current	I <sub>CC</sub>	$V_{CC} = 5.5V$	-	-	13	mA

**2.** Not more than one output should be shorted at a time, nor for more than 1 second.



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### AC Electrical Characteristics<sup>4</sup> $V_{cc} = 5V$ , $T_{J} = -55^{\circ}C$ to 125°C unless otherwise specified

PARAMETER	SYMBOL CONDITIONS		LIMITS			
	STMBOL	STIMBOL SONDITIONS		ТҮР	MAX	UNITS
Input Clock Frequency, CK <sub>A</sub>	f <sub>max</sub>		32	-	-	MHz
Input Clock Frequency, CK <sub>B</sub>	Imax	$C_{L} = 50 pF, R_{L} = 510 \Omega$	16	-	-	MHz
Fall, Rising Edge	t <sub>f</sub> , t <sub>r</sub>		-	-	2	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{A}} \text{ to } \text{Q}_{\text{A}} \end{array}$	t <sub>PLH</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	16	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{A}} \text{ to } \text{Q}_{\text{A}} \end{array}$	t <sub>PHL</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	18	
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{A}} \text{ to } \text{Q}_{\text{D}} \end{array}$	t <sub>PLH</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	70	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{A}} \text{ to } \text{Q}_{\text{D}} \end{array}$	t <sub>PHL</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	70	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{B}} \end{array}$	t <sub>PLH</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	16	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{B}} \end{array}$	t <sub>PHL</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	21	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{C}} \end{array}$	t <sub>PLH</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	32	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{C}} \end{array}$	t <sub>PHL</sub>	$C_L = 50 pF, R_L = 510 \Omega$	-	-	35	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{D}} \end{array}$	t <sub>PLH</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	-	-	51	ns
$\begin{array}{c} \text{Propagation Delay,} \\ \text{CK}_{\text{B}} \text{ to } \text{Q}_{\text{D}} \end{array}$	t <sub>PHL</sub>	$C_L = 50 pF, R_L = 510 \Omega$	-	-	51	ns
Propagation Delay, R0 to any output	t <sub>PHL</sub>	$C_L = 50 pF, R_L = 510 \Omega$	-	-	32	ns

## Timing Requirements<sup>4</sup> $V_{CC} = 5V$ , $T_{J} = -55^{\circ}C$ to 125°C unless otherwise specified

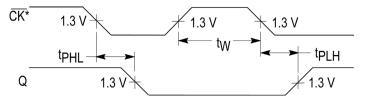
PARAMETER	SYMBOL	MBOL CONDITIONS	LIMITS			UNITS
	OTMEOL		MIN	TYP	MAX	- Chille
CK <sub>A</sub> Pulse Width		C <sub>L</sub> = 50pF, R <sub>L</sub> = 510Ω	15	-	-	ns
CK <sub>B</sub> Pulse Width	t <sub>w</sub>		30	-	-	ns
R0 Pulse Width			15	-	-	ns
Recovery Time, R0 to CK	t <sub>REC</sub>	$C_{L} = 50 pF, R_{L} = 510 \Omega$	25	-	-	ns

4. Not production tested in die form, characterized by chip design.

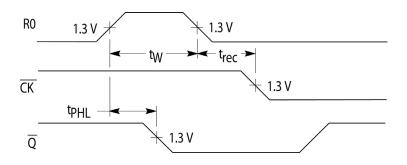


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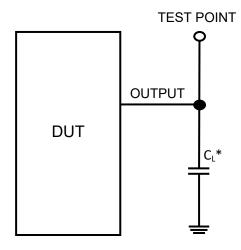
### Switching Waveforms



\* The number of Clock Pulses required between the t<sub>PHL</sub> and t<sub>PLH</sub> measurements can be determined from the Truth Table.



#### **Test Circuit**



\* Includes all probe and jig capacitance

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\* Includes all probe and jig capacitance

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