#### Hex D-type Flip-Flop in bare die form

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#### Description

The 54ALS174 Hex D-type Flip-Flop is fabricated using a 2µm 40V Bipolar process. The device is comprised of six flip-flops each having independent data input and data output. Load and clear is simultaneous, triggered by common clock and master reset respectively. D-Input levels transfer to Q output with the positive clock pulse.

#### Features:

- High speed 2ns (Min) propagation delay
- Full Military Temperature Range.
- Direct drop-in replacement for obsolete components in long term programs.

#### **Ordering Information**

The following part suffixes apply:

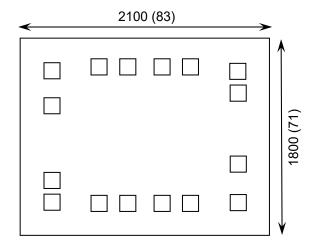
- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection+ MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)
   + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

#### Die Dimensions in µm (mils)



#### **Supply Formats:**

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

#### **Mechanical Specification**

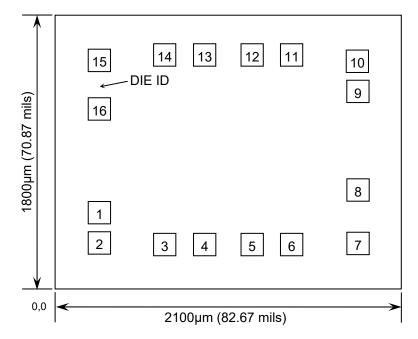
Die Size (Unsawn)	2100 x 1800 83 x 71	µm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils	
Top Metal Composition	Al 1%Si 1.1μm		
Back Metal Composition	N/A – Bare Si		





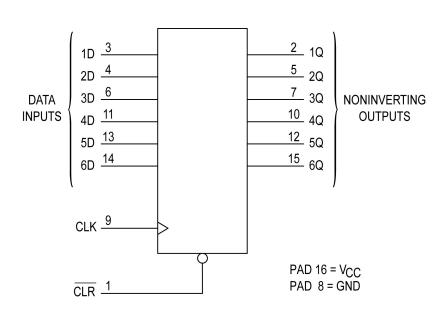
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## Pad Layout and Functions



PAD	FUNCTION	COORDINA	ATES (mm)			
PAD	FUNCTION	X	Υ			
1	CLR	0.200	0.435			
2	1Q	0.200	0.240			
3	1D	0.600	0.200			
4	2D	0.840	0.200			
5	2Q	1.130	0.200			
6	3D	1.370	0.200			
7	3Q	1.770	0.240			
8	GND	1.770	0.590			
9	CLK	1.770	1.240			
10	4Q	1.770	1.435			
11	4D	1.370	1.470			
12	5Q	1.130	1.470			
13	5D	0.840	1.470			
14	6D	0.600	1.470			
15	6Q	0.200	1.435			
16	V <sub>CC</sub>	0.200	1.120			
CONNECT CHIP BACK TO GND						

#### Logic Diagram



#### **Function Table**

	INPUTS	OUTPUT	
CLR	CLK	D	Q
L	X	X	L
Н		Н	Н
Н		L	L
Н	L	X	Q0

H = High level (steady state)

L = Low level (steady state)

\_─ = Low-to-High clock transition

X = Don't care





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V <sub>CC</sub>	7.0	V
DC Input Voltage	V <sub>IN</sub>	7.0	V
Storage Temperature Range	T <sub>STG</sub>	-65 to 150	°C

<sup>1.</sup> Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

#### **Recommended Operating Conditions**

	<u> </u>			
PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
High-Level Input Voltage	V <sub>IH</sub>	2	-	V
Low-Level Input Voltage	V <sub>IL</sub>	-	0.8	V
High-Level Output Current	I <sub>OH</sub>	-	-0.4	mA
Low-Level Output Current	I <sub>OL</sub>	-	4	mA
Operating Temperature Range	T <sub>J</sub>	-55	+125	°C

## DC Electrical Characteristics<sup>2</sup> T<sub>J</sub> = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		UNITS			
TANAMETER		CONDITIONS	MIN	TYP	MAX	GIALLO	
Minimum High-Level Input Voltage	V <sub>IH</sub>	-	2	-	-	V	
Maximum Low-Level Input Voltage	V <sub>IL</sub>	-	-	-	0.8	V	
Input Clamp Diode Voltage	V <sub>IK</sub>	$V_{CC} = MIN$ $I_{IN} = -18mA$	-	-	-1.5	V	
Output Voltage High	V <sub>OH</sub>	$V_{CC} = 4.5V \text{ to } 5.5V,$ $I_{OH} = -0.4\text{mA}$	V <sub>CC</sub> -2	-	-	V	
Output Voltage Low	V <sub>OL</sub>	V <sub>CC</sub> = 4.5V	-	0.25	0.4	V	
Input Current	I <sub>IN</sub>	$V_{CC} = 5.5V, V_{IN} = 7V$	-	-	0.1	mA	
Input High Current	I <sub>IH</sub>	$V_{CC} = 5.5V, V_{IN} = 2.7V$	-	-	20	μA	
Input Low Current	I <sub>IL</sub>	$V_{CC} = 5.5, V_{IN} = 0.4V$	-	-	-0.1	mA	
Output Current <sup>3</sup>	Io	$V_{CC} = 5.5, V_{OUT} = 2.25V$	-20	-	-112	mA	
Power Supply Current (Total)	I <sub>CC</sub>	V <sub>CC</sub> = 5.5V , V <sub>IN</sub> = 4.5V	-	11	19	mA	

**<sup>2</sup>**. All typical values @  $V_{CC}$  = 5V,  $T_J$  = 25°C.

<sup>3.</sup> Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, Ios





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## AC Electrical Characteristics <sup>4</sup> T<sub>J</sub> = -55°C to 125°C unless otherwise specified

PARAMETER	PARAMETER	SYMBOL	OL Voc	V <sub>cc</sub> CONDITIONS		LIMI <sup>*</sup>	ΓS	UNITS
	01111202	• 66	CONDITIONS	MIN	TYP	MAX	J. J	
Maximum Clock Frequency	f <sub>max</sub>	5V ±10%	$C_L = 50 pF,$ $R_L = 500 \Omega$	40	-	-	MHz	
Maximum Propagation Delay, CLR to Q (Figure 1)	t <sub>PLH,</sub>	$C_L = 50 pF,$ $R_L = 500 Ω$		3	-	20	ns	
	t <sub>PHL</sub>		5	-	30			
Maximum Propagation Delay, CLK to Q (Figure 1)	t <sub>PLH,</sub>	5V ±10%	C <sub>L</sub> = 50pF,	3	-	20	ns	
	t <sub>PHL</sub>	3. 210%	$R_L = 500\Omega$	5	-	24		

## Timing Requirements<sup>4</sup> T<sub>J</sub> = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	SYMBOL V <sub>cc</sub>	CONDITIONS	LIMITS			UNITS
	01111B0E	*66		MIN	TYP	MAX	J. Gittiro
Minimum Pulse Width, CLK (Figure 3)	$t_{w(H),} t_{w(L),}$	5V ±10%	$C_L = 50 pF$ , $R_L = 500 \Omega$	12.5	-	-	ns
Minimum Pulse Width, CLR (Figure 3)	t <sub>w(L)</sub>	5V ±10%	$C_L = 50 pF$ , $R_L = 500 \Omega$	15	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t <sub>su</sub>	5V ±10%	Data, $C_L = 50 pF$ , $R_L = 500 \Omega$	15	-	-	ns
Minimum Setup Time Before CLK (Figure 2)	t <sub>su</sub>	5V ±10%	$\overline{\text{CLR}}$ Inactive, $C_L = 50\text{pF}$ , $R_L = 500\Omega$	8	-	-	ns
Hold Time, Data after CLK (Figure 2)	t <sub>h</sub>	5V ±10%	$C_L = 50 pF$ , $R_L = 500 \Omega s$	0	-	-	ns

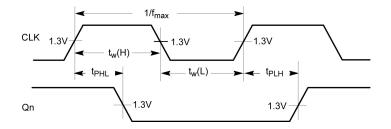
**<sup>4</sup>**. Not production tested in die form, characterized by chip design and tested in package.





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#### Switching Waveform



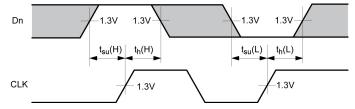


Figure 1 – Propagation Delay
Clock to Output and minimum Clock Frequency

Figure 2 - Data Setup and Hold Times

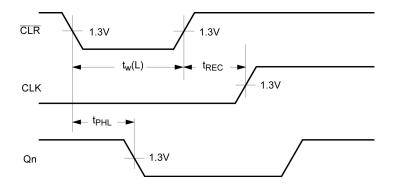
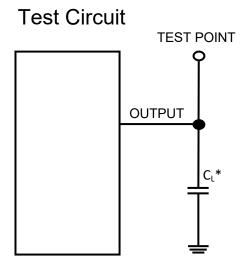


Figure 3 – Reset to Output, Reset to Clock Recovery



\* Includes all probe and jig capacitance

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