



Advanced High Speed CMOS Logic - 54AHC595

8-bit shift registers with 3-state output latches in bare die form

Rev 1.0
26/02/26

Description

The 54AHC595 is an 8-bit serial-in to parallel-out shift register which drives an 8-bit D-type latch with 3-state outputs. Both register and latch have independent positive triggered clock inputs. All registers capture data on rising edge and change output on the falling edge. If both clocks are connected together the input shift register is always one clock cycle ahead of the output register. The shift register also features asynchronous reset. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Features:

- High Frequency: 90 MHz (Min) $V_{CC} = 5V$, $C_L = 15pF$
- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 0.1µA
- Outputs directly interface CMOS, NMOS and TTL
- CMOS High Noise Immunity
- Function compatible with 54LS595
- Performance upgrade for 54AC595, 54HC595
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

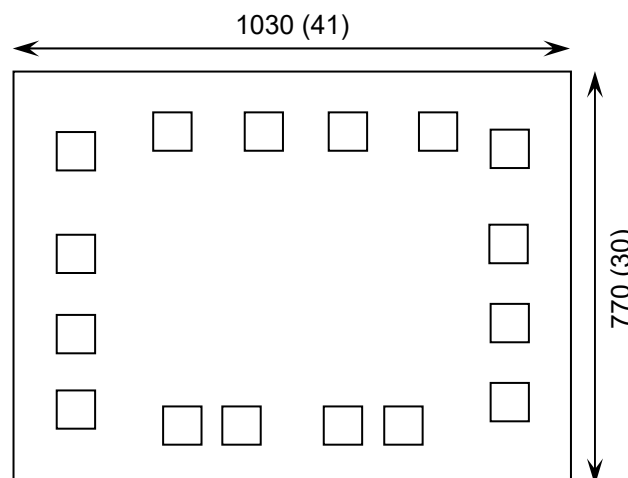
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space)
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- Assembled into Ceramic Package – On request

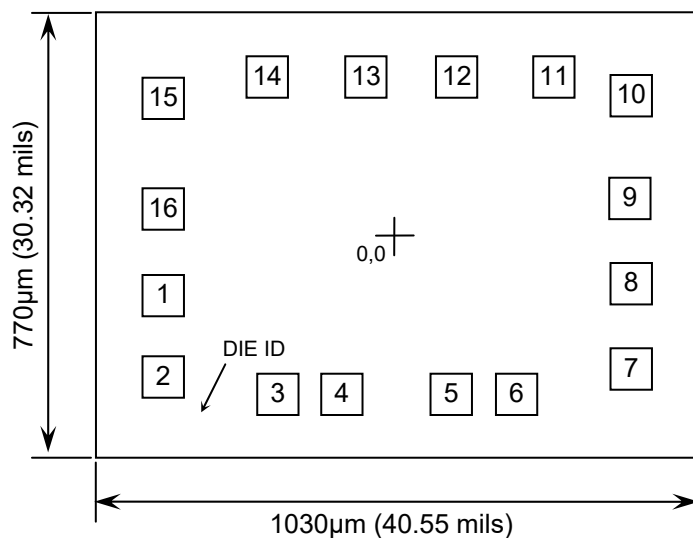
Mechanical Specification

Die Size (Unsawn)	1030 x 770 41 x 30	µm mils
Minimum Bond Pad Size	70 x 70 2.76 x 2.76	µm mils
Die Thickness	280 (±10) 11.02 (±0.39)	µm mils
Top Metal Composition	Al-Si-Cu 2.8 µm	
Back Metal Composition	N/A – Bare Si	





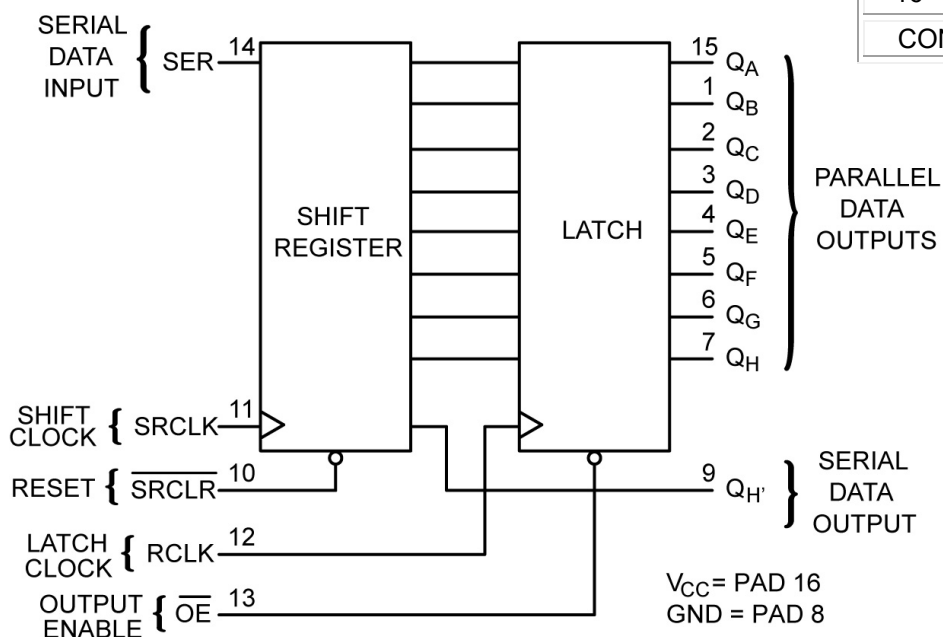
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	Q _B	-401.8	-102
2	Q _C	-401.8	-246
3	Q _D	-205.8	-273
4	Q _E	-95.8	-273
5	Q _F	95.8	-273
6	Q _G	205.8	-273
7	Q _H	401.8	-230.2
8	GND	401.8	-84.6
9	Q _{H'}	401.8	62.6
10	$\overline{\text{SRCLR}}$	401.8	243.2
11	SRCLK	272	273
12	RCLK	103.2	273
13	$\overline{\text{OE}}$	-54.4	273
14	SER	-233.2	273
15	Q _A	-401.8	237.6
16	V _{CC}	-401.8	46

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram





Function Table¹

INPUTS					OUTPUTS		FUNCTION
SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	Q_H'	Q_N	
X	X	L	L	X	L	NC	LOW level on $\overline{SRCLR}$ only affects the shift registers
X	↑	L	L	X	L	L	Empty shift-register loaded into storage register
X	X	H	L	X	L	Z	Shift-register clear. Parallel outputs in high- impedance OFF-state
↑	X	L	H	H	Q_G'	NC	Logic high level shifted into shift register stage 0. Content of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q_6') appears on serial output(Q_H')
X	↑	L	H	X	NC	Q_n'	Contents of shift register stages (internal Q_n') transfers to the storage register and parallel output stages
↑	↑	L	H	X	Q_G'	Q_n'	Shift register contents shifted through. Previous shift register content transfers to storage register & parallel output stages.

1. H=HIGH voltage level; L=LOW voltage level; ↑ =LOW-to-HIGH transition; Z=high-impedance OFF-state; NC=no change; X=don't care.

Absolute Maximum Ratings²

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to +7.0	V
DC Output Voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC V_{CC} or GND Current	I_{CC}	±75	mA
Power Dissipation in Still Air ³	P_D	500	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

2. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 3. Measured in plastic SOP-16 package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions⁴ (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V _{CC}	2	5.5	V
DC Input or Output Voltage		V _{IN} , V _{OUT}	0	V _{CC}	V
Operating Temperature Range		T _J	-55	+125	°C
Input Transition Rise or Fall Rate	V _{CC} = 3.3V ± 0.3V	Δt/Δv	0	100	ns/V
	V _{CC} = 5V ± 0.5V		0	20	ns/V

4. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.





DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum High-Level Input Voltage	V _{IH}	2.0V	V _{OUT} = 0.1V or V _{CC} - 0.1V I _{OUT} ≤ 20μA	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V _{IL}	2.0V	V _{OUT} = 0.1V or V _{CC} - 0.1V I _{OUT} ≤ 20μA	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V _{OH}	2.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 50μA	1.9	1.9	1.9	V
		3.0V		2.9	2.9	2.9	
		4.5V		4.4	4.4	4.4	
		3.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4mA	2.58	2.48	2.40	V
		4.5V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 8mA	3.94	3.80	3.70	
Maximum Low-Level Output Voltage	V _{OL}	2.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 50μA	0.1	0.1	0.1	V
		3.0V		0.1	0.1	0.1	
		4.5V		0.1	0.1	0.1	
		3.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4mA	0.36	0.44	0.55	V
		4.5V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 8mA	0.36	0.44	0.55	
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±2.0	μA
Maximum Three-State Leakage Current	I _{OZ}	5.5V	High-Impedance Output State, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = V _{CC} or GND	±0.25	±2.5	±10	μA
Maximum Quiescent Supply Current	I _{CC}	5.5V	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA	4	40	80	μA

5. -55°C ≤ T_J ≤ +125°C

AC Electrical Characteristics⁶ (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum Clock Frequency (Figure 5)	f _{min}	3.3V ±0.3V	C _L = 15pF	80	60	50	MHz
			C _L = 50pF	55	40	30	
		5V ±0.5V	C _L = 15pF	135	110	90	
			C _L = 50pF	95	85	70	

6. Not production tested in die form, characterized by chip design and tested in package.





AC Electrical Characteristics⁶ Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Maximum Propagation delay from input RCLK to output Q _A -Q _H (Figure 3,5)	t _{PLH} , t _{PHL}	3.3V ±0.3V	C _L = 15pF	13	14	16	ns
			C _L = 50pF	16	17.2	19	
		5V ±0.5V	C _L = 15pF	9	10	11	
			C _L = 50pF	11	12	13	
Maximum Propagation delay from input SRCLK to output QH' (Figure 3, 5)	t _{PLH} , t _{PHL}	3.3V ±0.3V	C _L = 15pF	13	15	16.5	ns
			C _L = 50pF	16.5	18.5	20.1	
		5V ±0.5V	C _L = 15pF	8.2	9.4	10.5	
			C _L = 50pF	11	11.4	13	
Maximum Propagation delay from input SRCLR to output QH' (Figure 3, 5)	t _{PHL}	3.3V ±0.3V	C _L = 15pF	12.8	13.7	15	ns
			C _L = 50pF	16.3	17.2	18.7	
		5V ±0.5V	C _L = 15pF	8	9.1	10	
			C _L = 50pF	10	11.1	12	
Maximum Propagation delay from input OE to output Q _A -Q _H (Figure 4, 5)	t _{PZH} , t _{PZL}	3.3V ±0.3V	C _L = 15pF	11.5	13.5	15	ns
			C _L = 50pF	15	17	18.5	
		5V ±0.5V	C _L = 15pF	8.6	10	11	
			C _L = 50pF	10.6	12	13	
	t _{PHZ} , t _{PLZ}	3.3V ±0.3V	C _L = 15pF	15.7	16.2	17.5	ns
			C _L = 50pF	10.3	11	12	
		5V ±0.5V	C _L = 15pF	15.7	16.2	17.5	
			C _L = 50pF	10.3	11	12	

Timing Requirements (Voltages referenced to GND)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			25°C	85°C	FULL RANGE ⁵	
Minimum pulse duration, SRCLK high or low (Figure 1,5)	t _w	3.3V ±0.3V	5	5	5	ns
		5V ±0.5V	5	5	5	
3.3V ±0.3V		5	5	5		
5V ±0.5V		5	5	5		
3.3V ±0.3V		5	5	5		
5V ±0.5V		5	5	5		
Minimum pulse duration, RCLK high or low (Figure 1, 5)						
Minimum pulse duration, SRCLR low (Figure 1,5)						





Timing Requirements Continued

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			25°C	85°C	FULL RANGE ⁵	
Minimum setup time, SER before SRCLK↑ (Figure 2,5)	t _{SU}	3.3V ±0.3V	3.5	3.5	3.5	ns
		5V ±0.5V	3	3	3	
Minimum setup time, SRCLK↑ before RCLK↑ (Figure 2,5)		3.3V ±0.3V	8	8	8	
		5V ±0.5V	5	5	5	
Minimum setup time, SRCLR low before RCLK↑ (Figure 2,5)		3.3V ±0.3V	8	8	8	
		5V ±0.5V	5	5	5	
Minimum setup time, SRCLR high(inactive) before SRCLK↑		3.3V ±0.3V	3	3	3	
		5V ±0.5V	2.5	2.5	2.5	
Minimum hold time, SER after SRCLK↑ (Figure 2,5)	t _H	3.3V ±0.3V	1.5	1.5	1.5	ns
		5V ±0.5V	2	2	2	

Operating Characteristics (V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Capacitance	C _{IN}	V _{IN} = V _{CC} or GND	-	3	10	pF
Output Capacitance	C _{OUT}	V _{OUT} = V _{CC} or GND	-	5.5	-	
Power Dissipation Capacitance ⁷	C _{PD}	No load, f = 1MHz	-	25.2	-	

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

Switching Waveforms

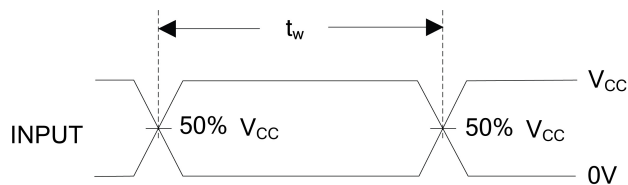


Figure 1 – Pulse duration

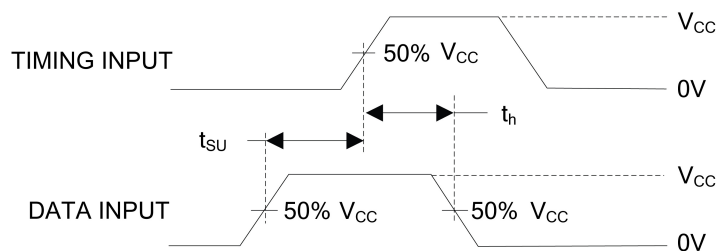


Figure 2 – Data setup and hold timing





Switching Waveforms continued

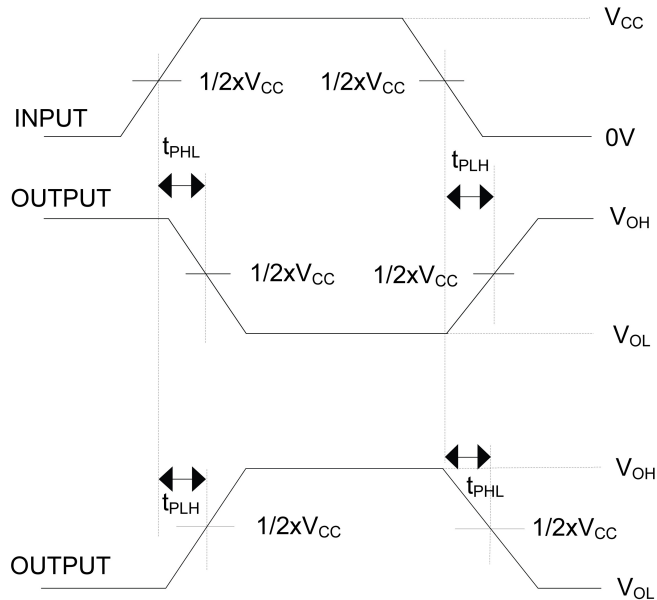


Figure 3 – Propagation delay timing

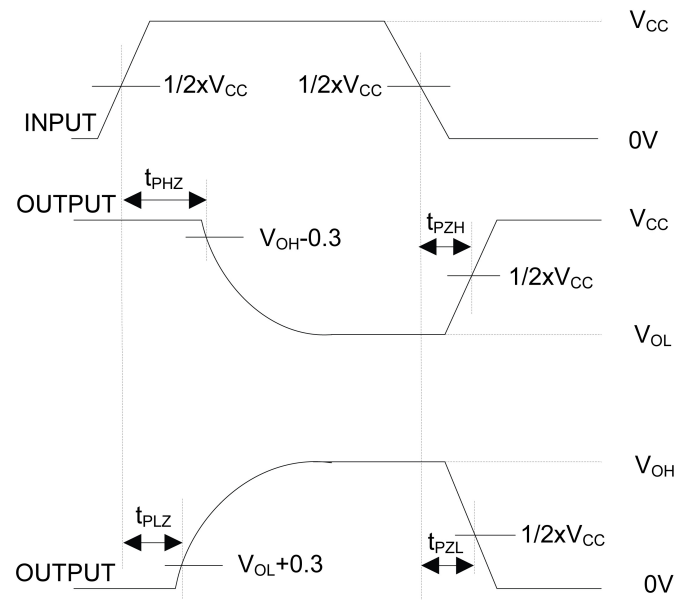
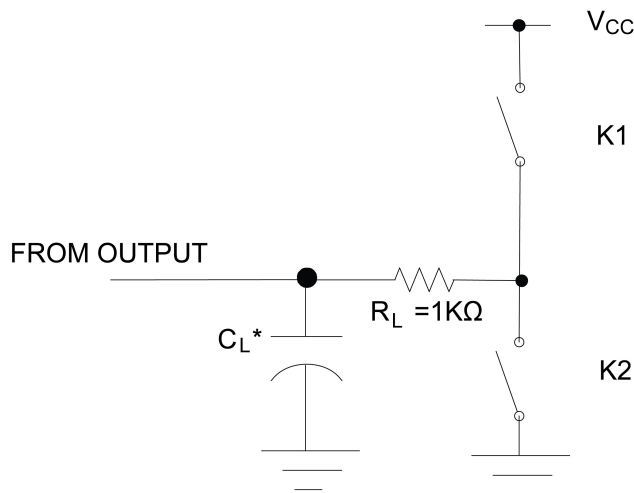


Figure 4 – 3-State enable & disable timing for $\overline{OE}$.



* Includes all probe and jig capacitance

Figure 5 – Load Circuit & Test Setup^{8, 9}

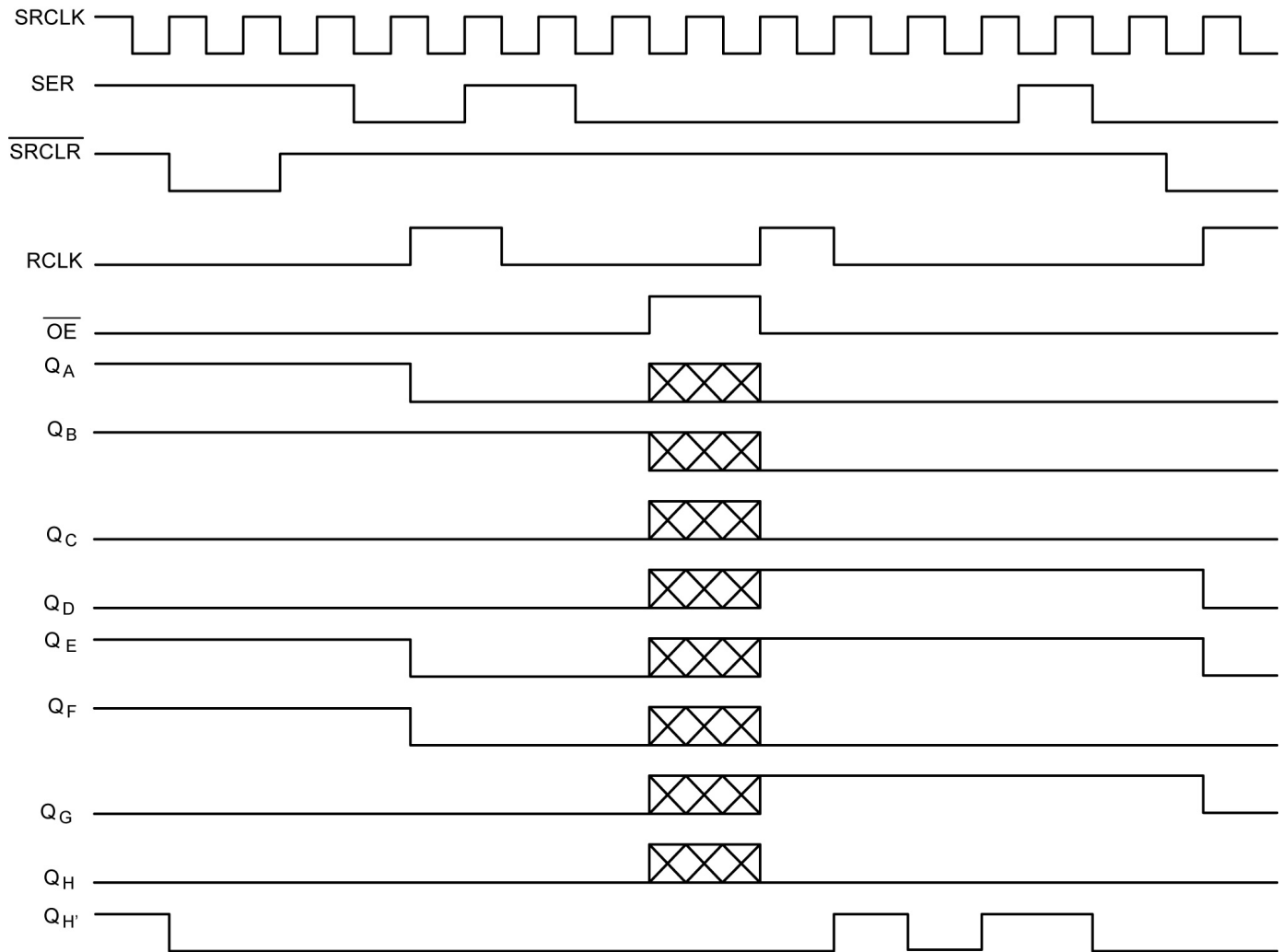
TEST	K1	K2
t_{PLH}, t_{PHL}	OPEN	OPEN
t_{PHZ}, t_{PZH}	OPEN	CLOSE
t_{PLZ}, t_{PZL}	CLOSE	OPEN

8. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_0 = 50\Omega$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$.
9. Outputs measured one at a time with one input transition per measurement.





Timing Diagram



NOTE: implies that the output is in a high-impedance state

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

