Advanced CMOS Logic – 54AC573

8-bit transparent D-Type Latch with 3-State Outputs in bare die form

Rev 1.0
19/3/2021

Description

The 54AC573 consists of eight D-type transparent latches fabricated using a 1.5µm 5V CMOS process to combine high speed performance LSTTL performance with CMOS low power consumption. Each latch is equipped with separate D-Type inputs and 3-State outputs for bus oriented applications. Data output changes asynchronously and data may be latched even when the outputs are not enabled. Inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors. Inputs are also equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Outputs Source/Sink 24mA
- Low input current: 1µA
- 3-State outputs
- Outputs directly interface CMOS, NMOS and TTL
- Operating voltage range: 2.0V to 6.0V
- Lower power consumption & higher speed
- Function compatible with 54HC573
- Full military temperature range.

Ordering Information

The following part suffixes apply:

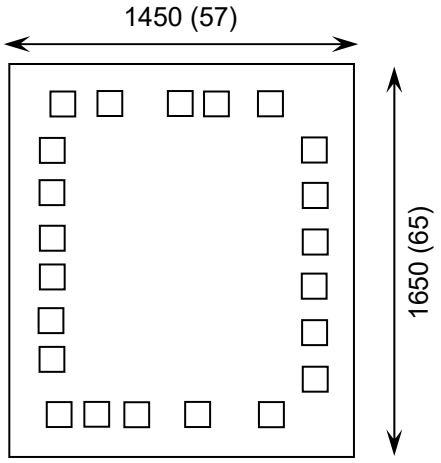
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1450 x 1650 57 x 65	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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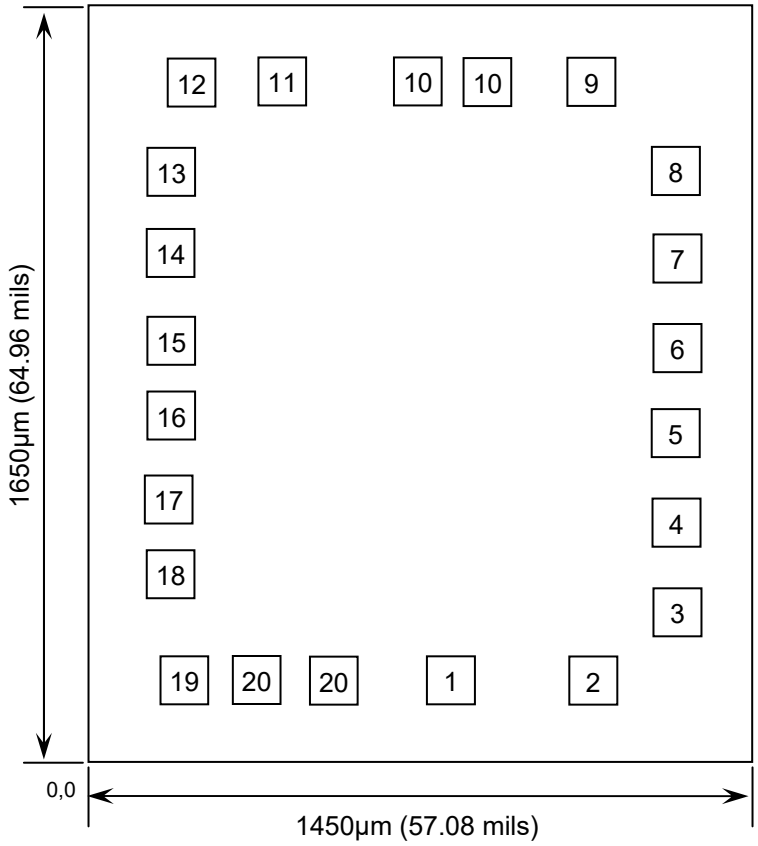
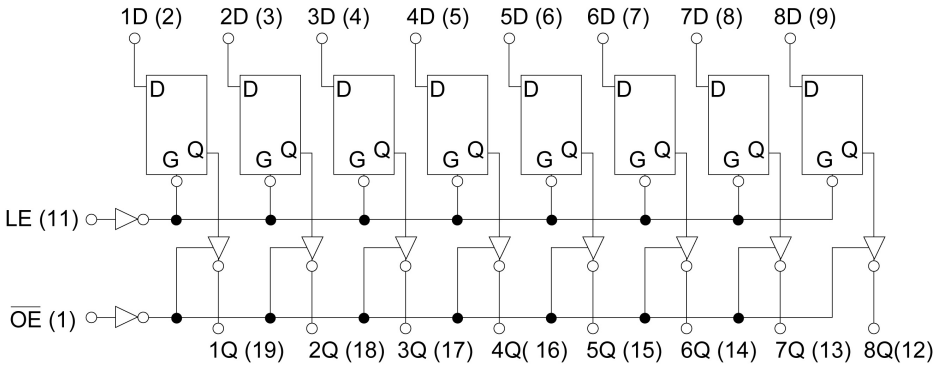
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{OE}$	0.735	0.100
2	1D	1.050	0.100
3	2D	1.23	0.280
4	3D	1.23	0.470
5	4D	1.23	0.660
6	5D	1.23	0.860
7	6D	1.23	1.050
8	7D	1.23	1.250
9	8D	1.050	1.430
10	GND	0.810	1.430
10	GND	0.660	1.430
11	LE	0.370	1.430
12	8Q	0.140	1.430
13	7Q	0.100	1.220
14	6Q	0.100	1.040
15	5Q	0.100	0.860
16	4Q	0.100	0.680
17	3Q	0.100	0.500
18	2Q	0.100	0.320
19	1Q	0.140	0.100
20	V_{CC}	0.320	0.100
20	V_{CC}	0.470	0.100
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 10 = GND, Pad 20 = V_{CC}

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2.0	6.0	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 30% to 70% V_{CC})	V_{CC} = 3.0V	Δt/ΔV	0	150	ns/V
	V_{CC} = 4.5V		0	40	
	V_{CC} = 5.5V		0	25	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V_{IL}	3.0V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.9	0.9	0.9	V
		4.5V		1.35	1.35	1.35	
		5.5V		1.65	1.65	1.65	

4. -55°C ≤ T_J ≤ +125°C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	3.0V	I_{OUT} = -50µA	2.9	2.9	2.9	V
		4.5V		4.4	4.4	4.4	
		5.5V		5.4	5.4	5.4	
		3.0V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -12 mA	2.56	2.46	2.40	
		4.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -24mA[5]	3.86	3.76	3.70	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -24mA[5]	4.86	4.76	4.70	
		5.5V	$V_{IN} = V_{IL}$ or V_{IH} I_{OH} = -50mA[6]	-	-	3.85	
Maximum Low-Level Output Voltage	V_{OL}	3.0V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		5.5V		0.1	0.1	0.1	
		3.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq$ 12mA	0.36	0.44	0.5	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq$ 24mA[5]	0.36	0.44	0.5	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq$ 24mA[5]	0.36	0.44	0.5	
		5.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert$ 50mA[6]	-	-	1.65	
Maximum Input Leakage Current	I_{IN}	5.5V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State Leakage Current	I_{OZ}	5.5V	$V_{OUT}=V_{CC}$ or GND $V_{IN} = V_{IL}$ or V_{IH}	±0.5	±2.5	±5	µA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	50	mA
	I_{OHD}	5.5V	V_{OHD} = 3.85V Min	-	-75	-50	
Maximum Quiescent Supply Current	I_{CC}	5.5V	$V_{IN} = V_{CC}$ or GND I_{OUT} = 0µA	8	80	160	µA

5. All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C **7.** Maximum test duration 2ms, one output loaded at a time

AC Electrical Characteristics[8] (V_{CC} 3.3V ±0.3V, V_{CC} 5V ±0.3V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay D to Q (Figure 1,5)	t_{PLH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	13.0	15.0	16.5	ns
		5.0V		10.0	11.5	13.0	
	t_{PHL}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	12.0	14.0	15.5	ns
		5.0V		9.5	11.0	12.5	
Maximum Propagation Delay LE to Q (Figure 2,5)	t_{PLH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	13.0	15.0	16.5	ns
		5.0V		9.5	11.0	12.5	
	t_{PHL}	3.3V		12.0	14.0	15.5	ns
		5.0V		8.5	10.0	11.5	
Output Enable Time OE to Q (Figure 3,6)	t_{PZH},	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	11.0	12.0	13.5	ns
		5.0V		9.0	10.0	11.5	
	t_{PZL}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	11.0	12.5	14.0	ns
		5.0V		8.5	9.5	11.0	
Output Enable Time OE to Q (Figure 3,6)	t_{PHZ}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	12.5	13.5	15.0	ns
		5.0V		11.0	12.0	13.5	
	t_{PLZ}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	9.5	10.5	12.0	ns
		5.0V		8.0	9.0	10.5	
Maximum Input Capacitance	C_{IN}	-	-	5.0	5.0	5.0	pF
Power Dissipation Capacitance[9]	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			
				25			pF

8. Not production tested in die form, characterized by chip design.
9. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6] (V_{CC} 3.3V ±0.3V, V_{CC} 5V ±0.3V)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to LE ,(Figure 2,4)	t_{SU}	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	3.5	4.0	5.0	ns
		5V		3.0	3.5	4.5	
Minimum Hold Time, LE to D, (Figure 2,4)	t_h	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	2.0	2.0	3.0	ns
		5V		2.0	2.0	3.0	
Minimum Pulse Width, LE, (Figure 2,4)	t_w	3.3V	C_L = 50pF, Input $t_r = t_f$ = 3ns	6.0	7.0	8.0	ns
		5V		4.0	5.0	6.0	

Switching Waveforms

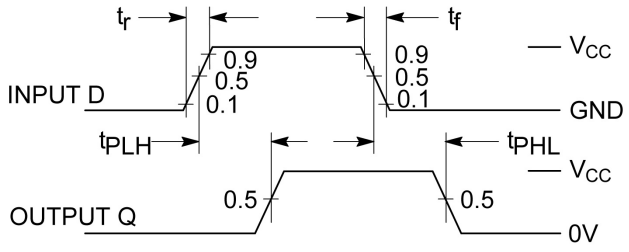


Figure 1 – Propagation Delay & Output Transition Time

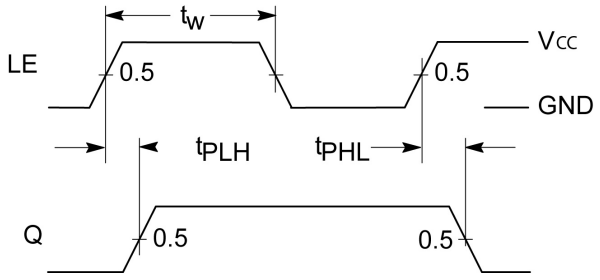


Figure 2 – Propagation Delay – Latch Enable to Q

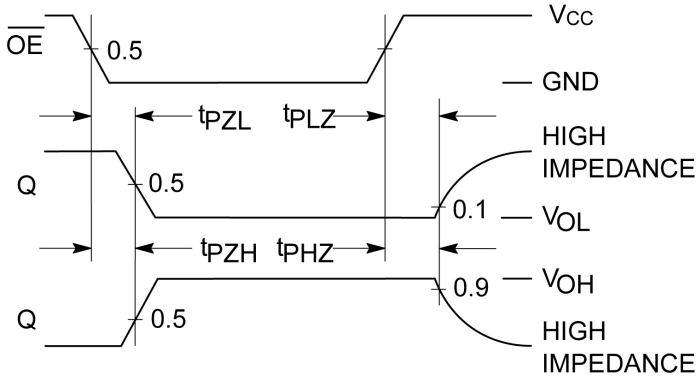


Figure 3 – Propagation Delay - Output Enable to Q

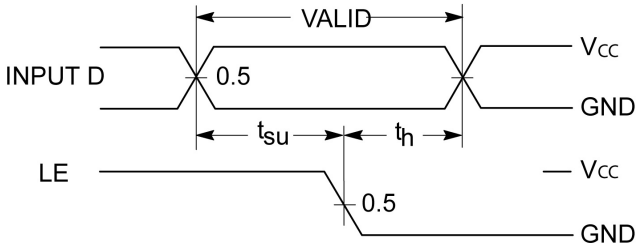
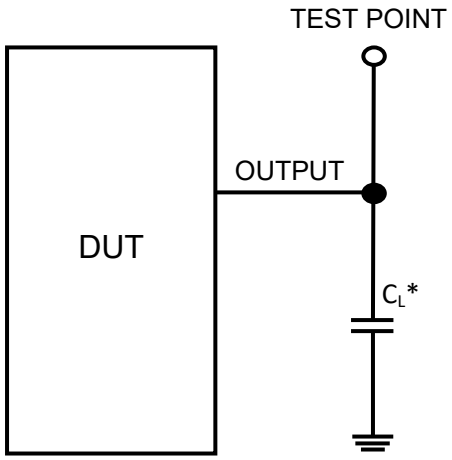


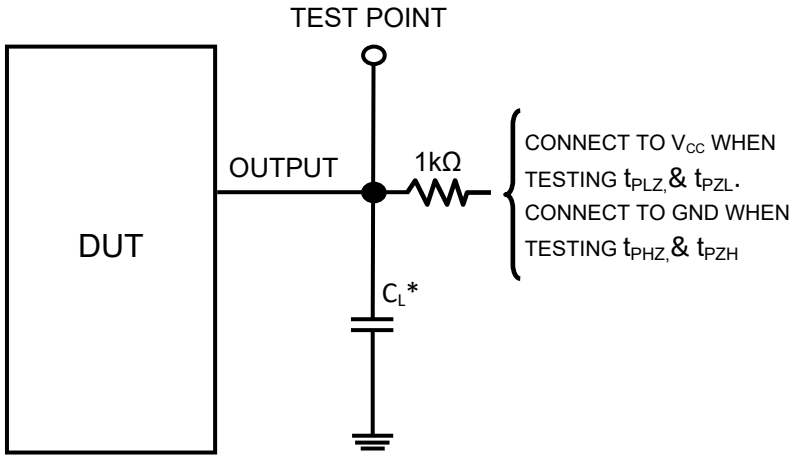
Figure 4 – Timing Requirements

Test Circuits



* Includes all probe and jig capacitance

Figure 5



* Includes all probe and jig capacitance

Figure 6