



Advanced CMOS Logic – 54AC244

Octal 3-State Non-Inverting Buffer / Line Driver / Line Receiver in bare die form

Rev 1.0
24/04/19

Description

The 54AC244 is produced on a 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device can be used as two 4-bit buffers or one 8-bit buffer & features non-inverting inputs with two output enables, each controlling four of the 3-state outputs. The device is designed to improve performance & density in clock drivers, 3-state memory address drivers & bus orientated transmitters and receivers. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} . Device inputs directly accept TTL without use of pull-up resistors.

Features:

- Outputs Source/Sink 24mA
- Low input current: 1µA
- 3-State outputs
- Outputs directly interface CMOS, NMOS and TTL
- Operating voltage range: 2.0V to 6.0V
- Lower power consumption & higher speed
- Function compatible with 54HC244
- Full military temperature range.

Ordering Information

The following part suffixes apply:

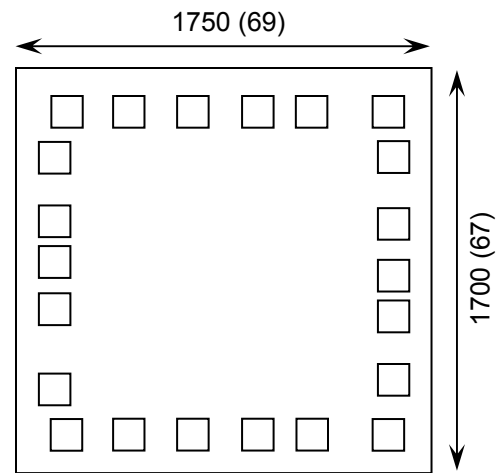
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space)
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1750 x 1700 69 x 67	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

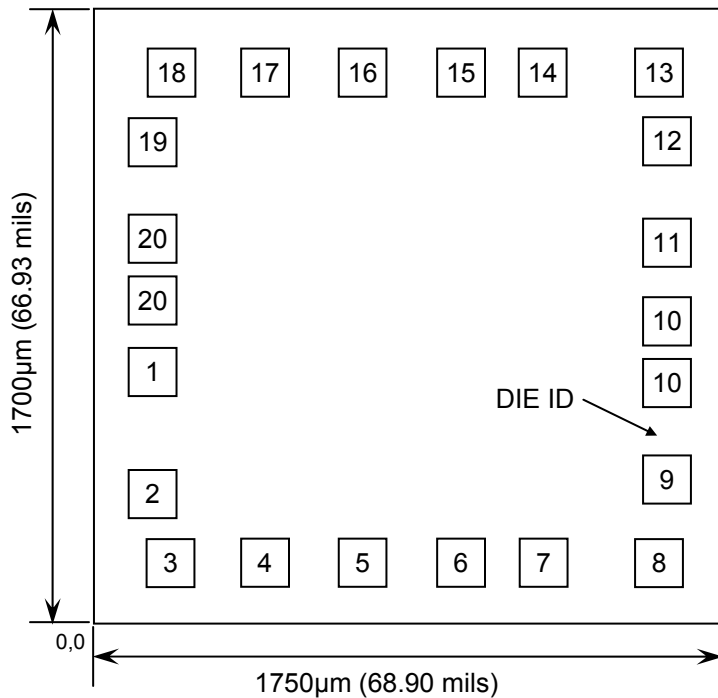




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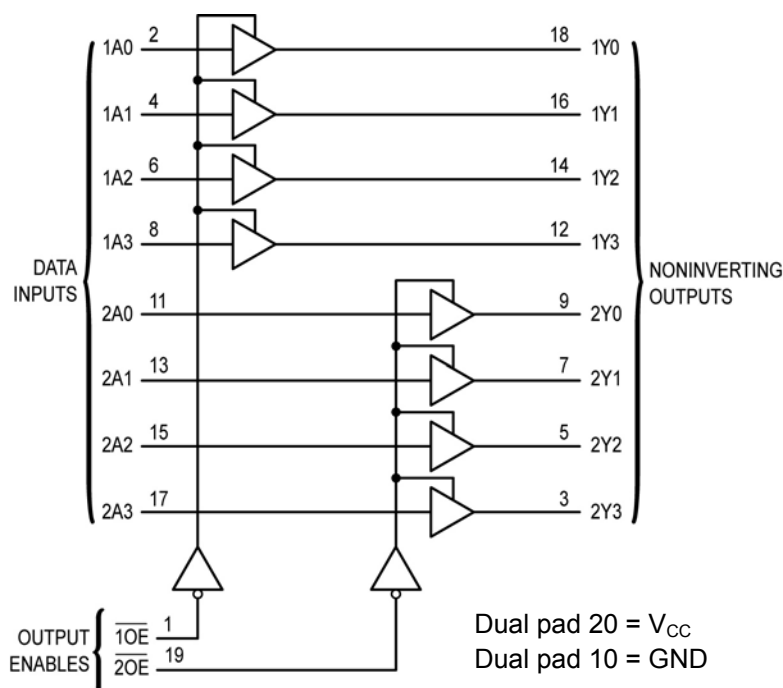
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1OE}$	0.100	0.630
2	1A0	0.100	0.290
3	2Y3	0.150	0.100
4	1A1	0.410	0.100
5	2Y2	0.680	0.100
6	1A2	0.950	0.100
7	2Y1	1.180	0.100
8	1A3	1.500	0.100
9	2Y0	1.520	0.330
10	GND	1.520	0.600
10	GND	1.520	0.770
11	2A0	1.520	0.990
12	1Y3	1.520	1.270
13	2A1	1.500	1.460
14	1Y2	1.180	1.460
15	2A2	0.950	1.460
16	1Y1	0.680	1.460
18	1Y0	0.150	1.460
19	$\overline{2OE}$	0.100	1.270
20	V _{CC}	0.100	1.000
20	V _{CC}	0.100	0.830

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram



Truth Table

INPUTS		OUTPUTS
$\overline{1OE}$ $\overline{2OE}$	1A, 2A	1Y, 2Y
L	L	L
L	H	H
H	X	Z

H = High level (steady state)
L = Low level (steady state)
X = Don't care, Z = High impedance





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Pad Descriptions

ADDRESS INPUTS

1A0, 1A1, 1A2, 1A3, 2A0, 2A1, 2A2, 2A3

(Pads 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

CONTROL INPUTS

1OE, 2OE (Pads 1, 19)

Output enables (active–low). When a low level is applied to these pins, the outputs are enabled and the devices function as non-inverting buffers. When a high level is applied, the outputs assume the high impedance state.

OUTPUTS

1Y0, 1Y1, 1Y2, 1Y3, 2Y0, 2Y1, 2Y2, 2Y3

(Pads 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output– enable pins, these outputs are either non-inverting outputs or high–impedance outputs.

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±50	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air ²	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	V_{CC}	2.0	6.0	V	
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V	
Operating Temperature Range	T_J	-55	+125	°C	
Output current - High	I_{OH}	-	-24	mA	
Output current - Low	I_{OL}	-	24	mA	
Input Rise or Fall rate (V_{IN} from 30% to 70% V_{CC})	$\Delta t/\Delta V$	$V_{CC} = 3.0V$	0	150	ns/V
		$V_{CC} = 4.5V$	0	40	
		$V_{CC} = 5.5V$	0	25	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.





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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Input Voltage	V _{IH}	3.0V	V _{OUT} = 0.1V or V _{CC} - 0.1V	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		5.5V		3.85	3.85	3.85	
Maximum Low-Level Input Voltage	V _{IL}	3.0V	V _{OUT} = 0.1V or V _{CC} - 0.1V	0.9	0.9	0.9	V
		4.5V		1.35	1.35	1.35	
		5.5V		1.65	1.65	1.65	
Minimum High-Level Output Voltage	V _{OH}	3.0V	I _{OUT} = -50μA	2.9	2.9	2.9	V
		4.5V		4.4	4.4	4.4	
		5.5V		5.4	5.4	5.4	
	V _{OH}	3.0V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OH} = -14mA	2.56	2.46	2.40	V
		4.5V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OH} = -24mA	3.86	3.76	3.70	
		5.5V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OH} = -24mA	4.86	4.76	4.70	
Maximum Low-Level Output Voltage	V _{OL}	3.0V	I _{OUT} = 50μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		5.5V		0.1	0.1	0.1	
	V _{OL}	3.0V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OL} = 12mA	0.36	0.44	0.50	V
		4.5V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OL} = 24mA	0.36	0.44	0.50	
		5.5V	V _{IN} = V _{IL} or V _{IH} ⁵ I _{OL} = 24mA	0.36	0.44	0.50	
Maximum Input Leakage Current	I _{IN}	5.5V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	μA
Maximum 3-State leakage current	I _{OZ}	5.5V	V _{OUT} = V _{CC} or GND V _{IN} = V _{IL} or V _{IH}	±0.5	±2.5	±5	μA
Minimum Dynamic Output Current ⁶	I _{OLD}	5.5V	V _{OLD} = 1.65V Max	-	75	50	mA
	I _{OHD}	5.5V	V _{OHD} = 3.85V Min	-	-75	-50	
Maximum Quiescent Supply Leakage Current	I _{CC}	5.5V	V _{IN} = V _{CC} or GND I _{OUT} = 0μA	8	40	80	μA

4. -55°C ≤ T_j ≤ +125°C 5. All outputs loaded; thresholds on input associated with output under test. 6. Maximum test duration 2.0 ms, one output loaded at a time.





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AC Electrical Characteristics⁷

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Propagation Delay 1A to 1Y or 2A to 2Y (Figure 1)	t _{PLH}	3.3V ±0.3	C _L = 50pF	9.0	10.0	12.5	ns
	t _{PHL}			9.0	10.0	12.0	
	t _{PLH}	5V ±0.5	C _L = 50pF	7.0	7.5	9.5	ns
	t _{PHL}			7.0	7.5	9.0	
Output Enable Time OE to 1Y or 2Y (Figure 2)	t _{PZH}	3.3V ±0.3	C _L = 50pF	10.5	11.0	11.5	ns
	t _{PZL}			10.0	11.0	13	
	t _{PZH}	5V ±0.5	C _L = 50pF	7.0	8.0	9.0	ns
	t _{PZL}			8.0	8.5	10.5	
Output Disable Time OE to 1Y or 2Y	t _{PHZ}	3.3V ±0.3	C _L = 50pF	10.0	10.5	12.5	ns
	t _{PLZ}			10.5	11.5	13.0	
	t _{PHZ}	5V ±0.5	C _L = 50pF	9	9.5	10.5	ns
	t _{PLZ}			9	9.5	11	

7. Not production tested in die form, characterized by chip design and tested in package.

Capacitance⁷

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	TYPICAL	UNITS
Maximum Input Capacitance	C _{IN}	5.0V	T _J = 25°C	4.5	pF
Power Dissipation Capacitance (Per Buffer/Driver)	C _{PD}	5.0V	T _J = 25°C, C _L = 50pF, F = 1MHz	45	pF

Switching Waveforms

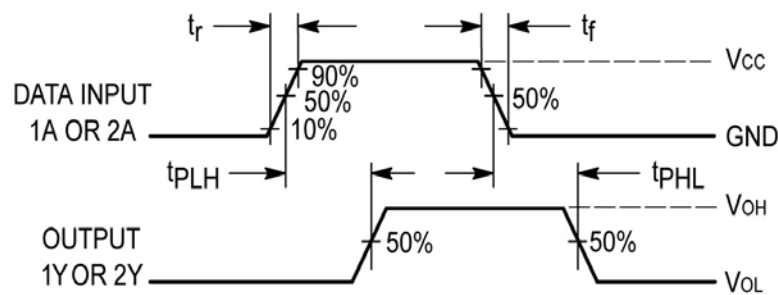


Figure 1 – Propagation Delay - Input 1A or 2A to Output 1Y or 2Y





Switching Waveforms continued

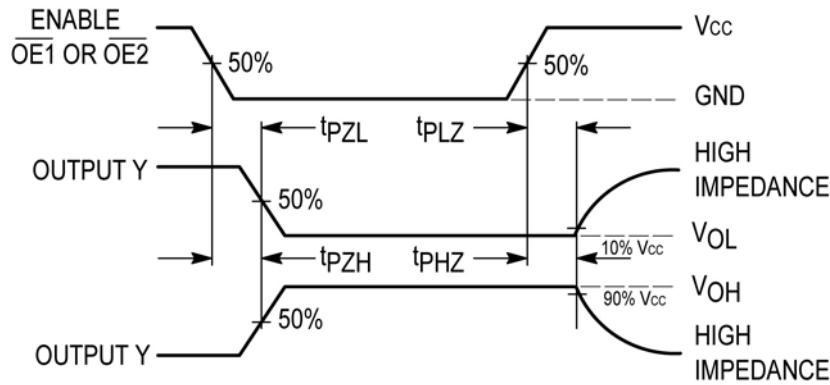
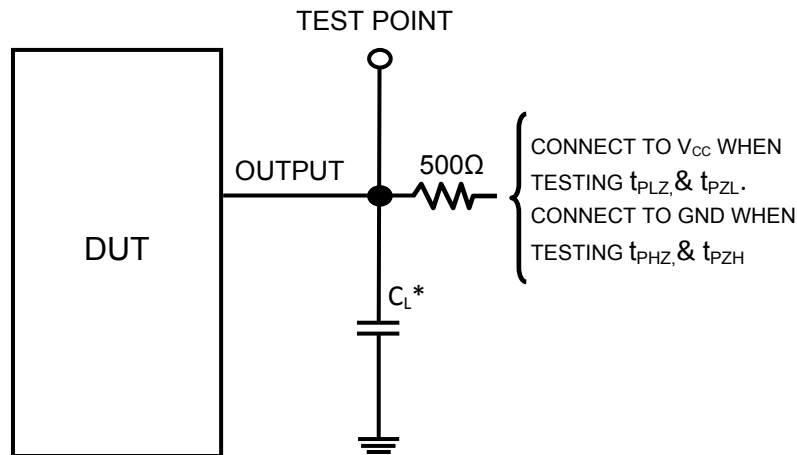


Figure 2 – Propagation Delay - Output Enable to Output 1Y or 2Y

Test Circuit



* Includes all probe and jig capacitance

Figure 3

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