



PNP Transistor Bare Die – 2N6107

Rev 1.1
22/04/24

Bipolar Power Transistor in bare die form
Complement to NPN 2N6292

Features:

- Collector current up to 7A
- High DC Current Gain, $h_{FE} = 30-150 @ I_C = 4A$
- Low $V_{CE(sat)} = 3.5V \text{ Max } @ I_C = 7A$
- Solderable back metal
- High Reliability tested grades for Military + Space

Ordering Information:

The following part suffixes apply:

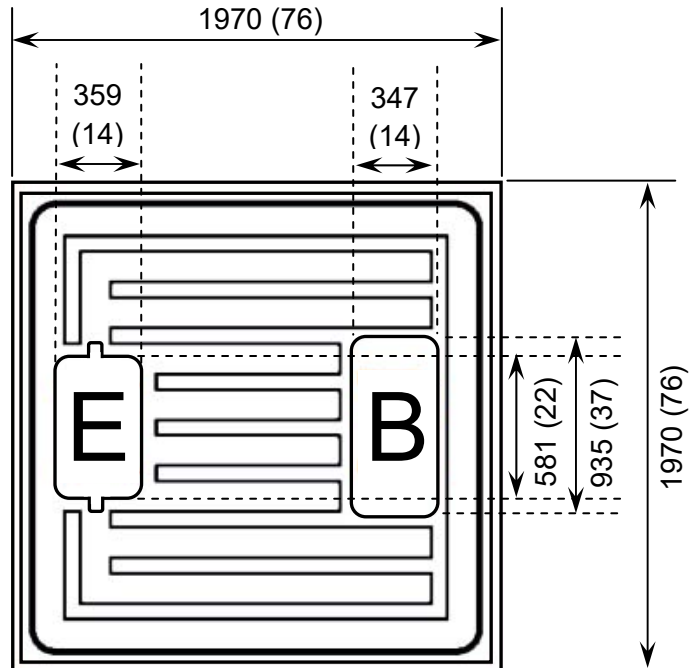
- No suffix - Commercial grade die
- "H" – Hi-rel grade die + MIL-STD-38534 Class H LAT
- "K" – Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

www.siliconsupplies.com/bare-die-lot-qualification

Die Dimensions in μm (mils)



DIE BACK = COLLECTOR

Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – Specific request
- Unsawn Wafer – Specific request
- With additional electrical selection – Specific request
- Sawn as pairs or adjacent pair pick – Specific request

Mechanical Specification

Die Size (Excluding Saw Street)	1970 x 1970 76 x 76	μm mils
Emitter Pad Size	359 x 581 14 x 22	μm mils
Base Pad Size	347 x 935 14 x 37	μm mils
Die Thickness	250 (± 25) 9.84 (± 1)	μm mils
Top Metal Composition	Al	
Back Metal Composition	Ti/Ni/Ag	





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Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage	V_{CEO}	70	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current - Continuous	I_C	7	A
Base Current	I_B	3	A
Operating Junction Temperature	T_J	-65 to 150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to 150	$^\circ\text{C}$

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_E = 0$	80	-	-	V
Collector-Emitter Sustaining Voltage ¹	$V_{CEO(SUS)}$	$I_B = 0, I_C = 100\text{mA}$	70	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_C = 0$	5	-	-	V
Collector Cut-off Current	I_{CEO}	$V_{CE} = 60\text{V}, I_B = 0$	-	-	1.0	mA
	I_{CEX}	$V_{CE} = 80\text{V}, V_{BE(off)} = 1.5\text{V}$	-	-	0.1	mA
	I_{CEX}^2	$V_{CE} = 70\text{V}, V_{BE(off)} = 1.5\text{V}, T_J = 125^\circ\text{C}$	-	-	2.0	mA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = 5\text{V}, I_C = 0$	-	-	1.0	mA
ON CHARACTERISTICS						
Forward-Current Transfer Ratio ¹	h_{FE}	$I_C = 2\text{A}, V_{CE} = 4\text{V}$	30	-	150	-
		$I_C = 7\text{A}, V_{CE} = 4\text{V}$	2.3	-	-	-
Collector-Emitter Saturation Voltage ¹	$V_{CE(sat)}$	$I_C = 7\text{A}, I_B = 3\text{A}$	-	-	3.5	V
Base-Emitter On Voltage ¹	$V_{BE(on)}$	$I_C = 7\text{A}, V_{CE} = 4\text{V}$	-	-	3.0	V
SMALL SIGNAL CHARACTERISTICS²						
Transition Frequency ³	f_T	$V_{CE} = 4\text{V}, I_C = 0.5\text{A}, f = 1\text{MHz}$	10	-	-	MHz
Small-Signal Current Gain	h_{fe}	$V_{CE} = 4\text{V}, I_C = 0.5\text{A}, f = 50\text{kHz}$	20	-	-	-

1. Pulsed duration = 300 μs , duty cycle $\leq 2\%$

2. Not production testing in die form, characterized by chip design and package verification

3. $f_T = |h_{fe}| \cdot f_{TEST}$

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