

Rev 1.0 12/07/23

**Darlington construction transistor in bare die form** Complement to PNP 2N6042

#### Features:

- Collector current up to 8A
- Very high current gain
- Enables high impedance circuitry
- Solderable Back Metal
- High Reliability tested grades for Military + Space

#### Ordering Information:

The following part suffixes apply:

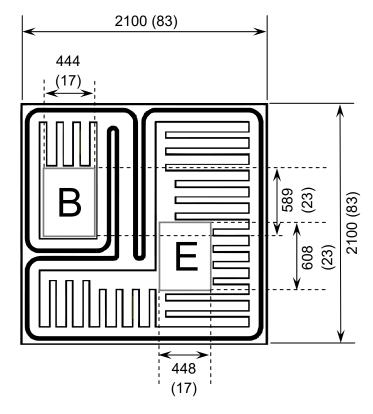
- No suffix Commercial grade die
- "H" Hi-rel grade die + MIL-STD-38534 Class H LAT
- "K" Hi-rel grade die + MIL-STD-38534 Class K LAT.

LAT = Lot acceptance Test.

For information on Hi-Rel LAT flows please see below.

www.siliconsupplies.com\bare-die-lot-qualification

### Die Dimensions in µm (mils)



**DIE BACK** = COLLECTOR

#### **Supply Formats:**

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape Specific request
- Unsawn Wafer Specific request
- With additional electrical selection Specific request
- Sawn as pairs or adjacent pair pick Specific request

#### **Mechanical Specification**

Die Size (Excluding Saw Street)	2100 x 2100 83 x 83	µm mils	
Base Pad Size	444 x 589 17 x 23	µm mils	
Emitter Pad Size	448 x 608 17 x 23	µm mils	
Die Thickness	260 (±20) 10 (±0.79)	µm mils	
Top Metal Composition	Al		
Back Metal Composition	Ti/Ni/Ag		





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## Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise stated

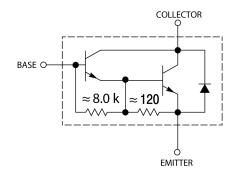
PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V <sub>CBO</sub>	100	V
Collector-Emitter Voltage	V <sub>CEO</sub>	100	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub>	8	A
Base Current	I <sub>B</sub>	120	mA
Junction Temperature	TJ	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C

## Electrical Characteristics T<sub>A</sub> = 25°C unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage	V <sub>(BR)CBO</sub>	I <sub>C</sub> = 100mA	100	-	-	V
Collector-Emitter Breakdown Voltage	V <sub>CEO(SUS)</sub>	I <sub>C</sub> = 30mA, I <sub>B</sub> = 0	100	-	-	V
Emitter-Base Breakdown Voltage	V <sub>(BR)EBO</sub>	I <sub>E</sub> = 100μA	5	-	-	V
Collector Cut-off Current	I <sub>CBO</sub>	$V_{CB} = 100V, I_{E} = 0$	-	-	500	μA
	I <sub>CEO</sub>	V <sub>CE</sub> = 50V, I <sub>B</sub> = 0	-	-	500	μA
Emitter Cut-off Current	I <sub>EBO</sub>	$V_{EB} = 5V, I_{C} = 0$	-	-	2	mA
ON CHARACTERISTICS						
DC Current Gain	h <sub>FE</sub>	$I_C = 3A$ , $V_{CE} = 4V$	1000	-	20000	-
		$I_{C} = 8A, V_{CE} = 4V$	100	-	-	-
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> = 3A, I <sub>B</sub> = 12mA	-	-	2	V
		I <sub>C</sub> = 8A, I <sub>B</sub> = 80mA	-	-	4	V
Base-Emitter Saturation Voltage	V <sub>BE(SAT)</sub>	I <sub>C</sub> = 8A, I <sub>B</sub> = 80mA	-	-	4.5	V
Base-Emitter On Voltage	V <sub>BE(ON)</sub>	I <sub>C</sub> = 4A, V <sub>CE</sub> = 4V	-	-	2.8	V
SMALL-SIGNAL CHARACTERISTICS <sup>1</sup>						
Small-Signal Current Gain	Ih <sub>fe</sub> l	V <sub>CE</sub> = 4V, I <sub>C</sub> = 3A, f = 1 MHz	4	-	-	-
Output Capacitance	C <sub>obo</sub>	V <sub>CB</sub> = 10V, I <sub>E</sub> = 1A, f = 0.1 MHz	-	-	300	pF
Small-Signal Current Gain	h <sub>fe</sub>	V <sub>CE</sub> = 4V, I <sub>C</sub> = 3A, f = 1 KHz	300	-	-	-

<sup>1.</sup> Not production testing in die form, characterized by chip design and tested in package.

## Internal NPN Schematic Diagram







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### **Typical Electrical Characteristics**

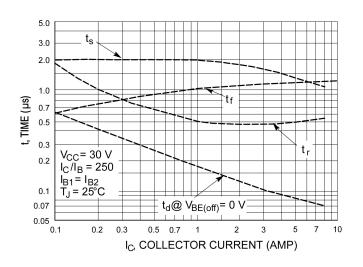


Figure 1 – Switching Times

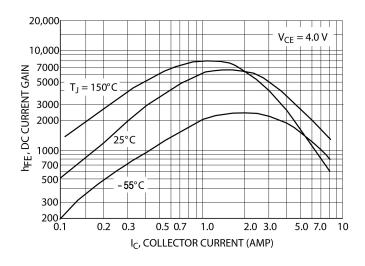


Figure 4 - DC Current Gain

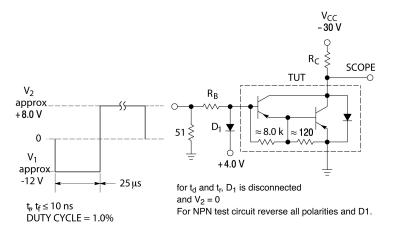


Figure 2 – Switching Times Test Circuit (PNP – follow notes for NPN)

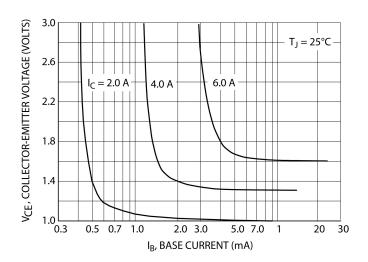


Figure 5 – Collector Saturation Region





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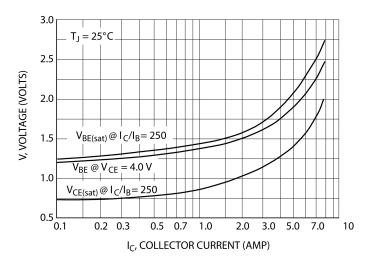


Figure 6 - "On" Voltages

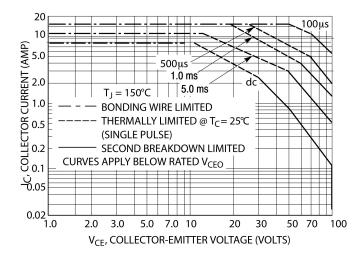


Figure 8 – Active-region Safe Operating Area

300 200 200 T<sub>J</sub> = 25°C T<sub>J</sub> = 25°C C<sub>ob</sub> T<sub>J</sub> = 25°C 70 50 50 0.1 0.2 0.5 1.0 2.0 5.0 10 20 50 100 V<sub>R</sub>, REVERSE VOLTAGE (VOLTS)

Figure 7 - Capacitance

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 8 is based on  $T_{J(pk)} = 150^{\circ} C$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^{\circ} C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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