



NPN Transistor Bare Die, 2N3903

Rev 1.0
02/09/17

General purpose amplifier or saturated switch in bare die form
Complement to PNP 2N3906

Features:

- Low Leakage Current 50nA Max
- Low Collector Output Capacitance 4pF Max
- Characterized at temperature extremes
- High Reliability Gold Back Metal
- High Reliability tested grades for Military + Space

Ordering Information:

The following part suffixes apply:

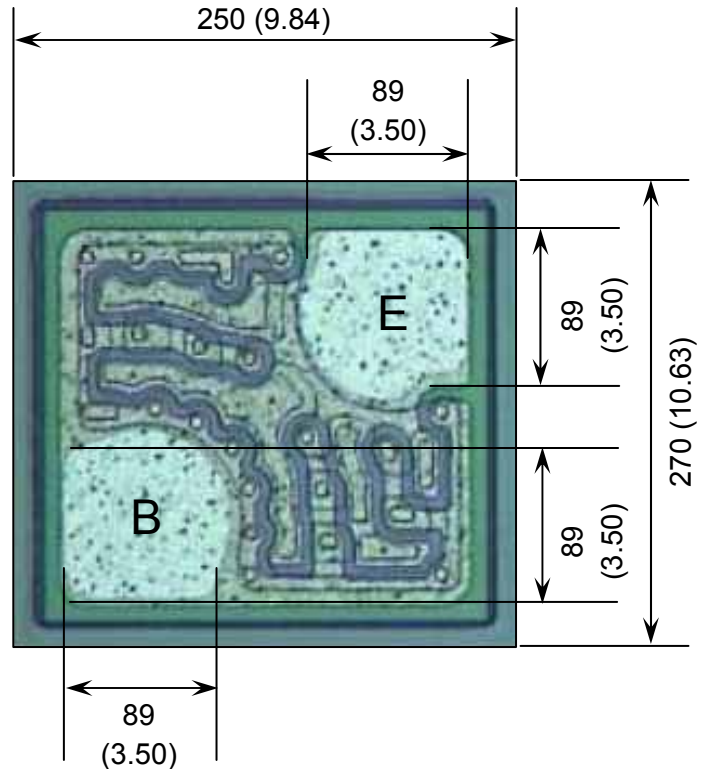
- No suffix - MIL-STD-750 /2072 Visual Inspection
- "H" - MIL-STD-750 /2072 Visual Inspection
+ MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-750 /2072 Visual Inspection
+ MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in μm (mils)



E = EMITTER **B** = BASE

DIE BACK = COLLECTOR

Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – Specific request
- Unsawn Wafer – Specific request
- With additional electrical selection – Specific request
- Sawn as pairs or adjacent pair pick – Specific request

Mechanical Specification

Die Size (Excluding Saw Street)	250 x 270 9.84 x 10.63	μm mils
Base Pad Size Emitter Pad Size	89 x 89 3.50 x 3.50	μm mils
Die Thickness	180 (± 20) 7.09 (± 0.79)	μm mils
Top Metal Composition	Al - 1.3 μm	
Back Metal Composition	AuAs - 0.9 μm	





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Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	VALUE	UNIT
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	40	V
Emitter-Base Voltage	V_{EBO}	6	V
Collector Current	I_C	200	mA
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 150	$^\circ\text{C}$

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise stated

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu\text{A}$	60	-	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{mA}$	40	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu\text{A}$	6	-	-	V
Collector Cut-off Current	I_{CEX}	$V_{CE} = 30\text{V}, V_{EB} = 3\text{V}$	-	-	50	nA
Base Cut-off Current	I_{BL}	$V_{CE} = 30\text{V}, V_{EB} = 3\text{V}$	-	-	50	nA
Emitter Cut-off Current	I_{EBO}	$V_{EB} = 5\text{V}$	-	-	50	nA
ON CHARACTERISTICS						
Forward-Current Transfer Ratio	h_{FE}	$V_{CE} = 1\text{V}, I_C = 0.1\text{mA}$	20	-	-	-
		$V_{CE} = 1\text{V}, I_C = 1\text{mA}$	35	-	-	-
		$V_{CE} = 1\text{V}, I_C = 10\text{mA}$	50	-	150	-
		$V_{CE} = 1\text{V}, I_C = 50\text{mA}$	30	-	-	-
		$V_{CE} = 1\text{V}, I_C = 100\text{mA}$	15	-	-	-
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 10\text{mA}, I_B = 1\text{mA}$	-	-	0.2	V
		$I_C = 50\text{mA}, I_B = 5\text{mA}$	-	-	0.3	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = 10\text{mA}, I_B = 1\text{mA}$	-	-	0.85	V
		$I_C = 50\text{mA}, I_B = 5\text{mA}$	-	-	0.95	V
SMALL SIGNAL CHARACTERISTICS¹						
Transition Frequency	f_T	$V_{CE} = 20\text{V}, I_E = -10\text{mA}$	250	-	-	MHz
Output Capacitance	C_{obo}	$V_{CB} = 5\text{V}, I_E = 0, f = 1\text{MHz}$	-	-	4	pF
Input Capacitance	C_{ibo}	$V_{EB} = 0.5\text{V}, I_C = 0, f = 1\text{MHz}$	-	-	8	
SWITCHING CHARACTERISTICS¹						
Delay Time	t_d	$V_{CC} = 3\text{V}, V_{BE} = 0.5\text{V}$ $I_C = 10\text{mA}, I_{B1} = 1\text{mA}$	-	-	35	ns
Rise Time	t_r		-	-	35	
Storage Time	t_s	$V_{CC} = 3\text{V}, I_C = 10\text{mA}$ $I_{B1} = I_{B2} = 1\text{mA}$	-	-	175	
Fall Time	t_f		-	-	50	

Note 1: Not production testing in die form, characterized by chip design and tested in package LAT.





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Typical Electrical Characteristics

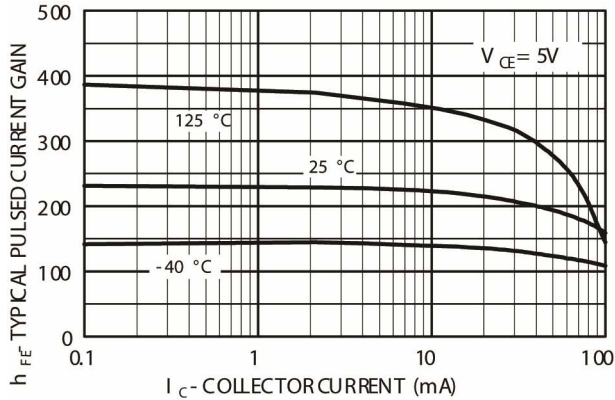


Fig 1 - Typical Pulsed Current Gain versus Collector Current

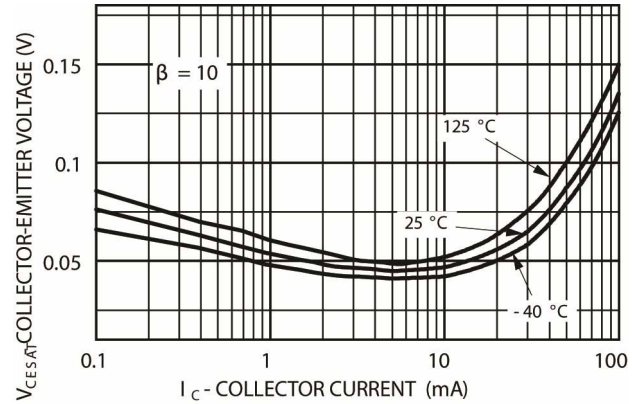


Fig 2 - Collector-Emitter Saturation Voltage versus Collector Current

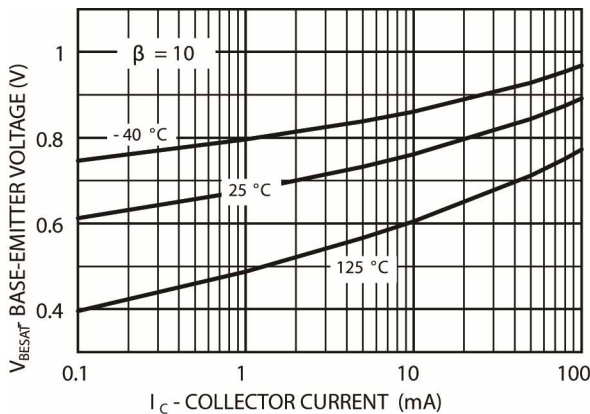


Fig 3 - Base-Emitter Saturation Voltage versus Collector Current

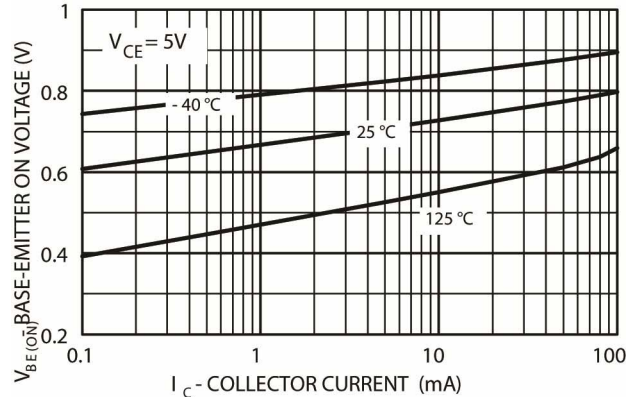


Fig 4 - Base-Emitter ON Voltage versus Collector Current

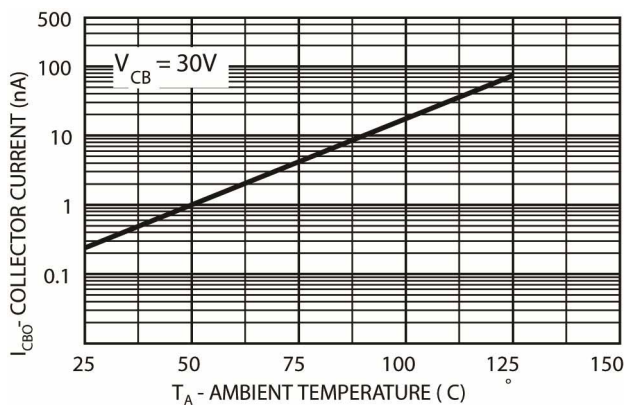


Fig 5 - Collector-Cut-off Current versus Ambient Temperature

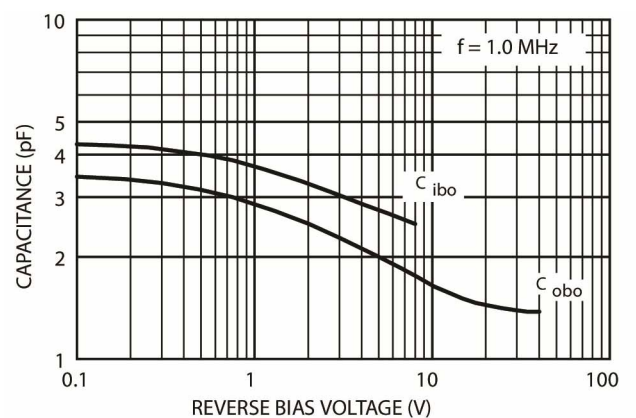


Fig 6 - Capacitance versus Reverse Bias Voltage





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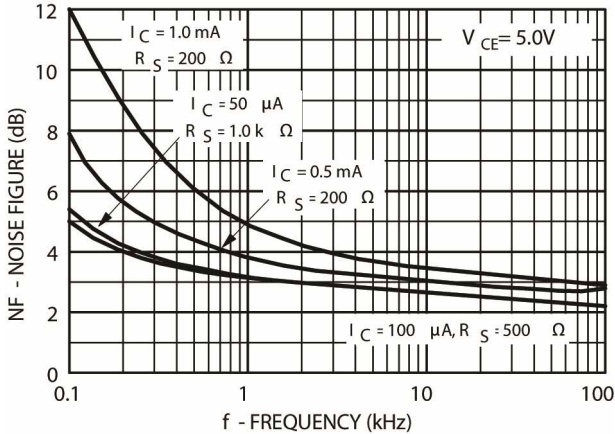


Fig 7 – Noise Figure versus Frequency

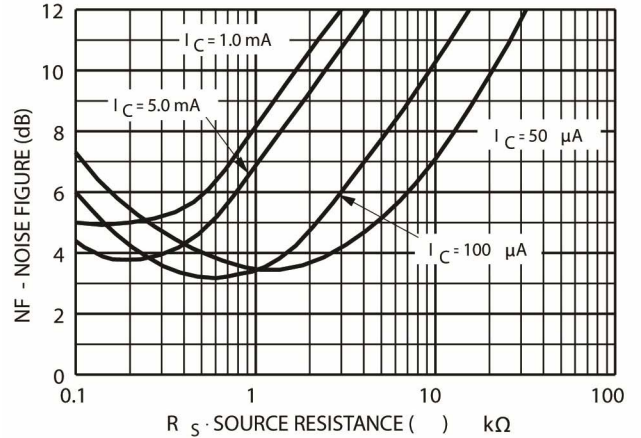


Fig 8 - Noise Figure versus Source Resistance

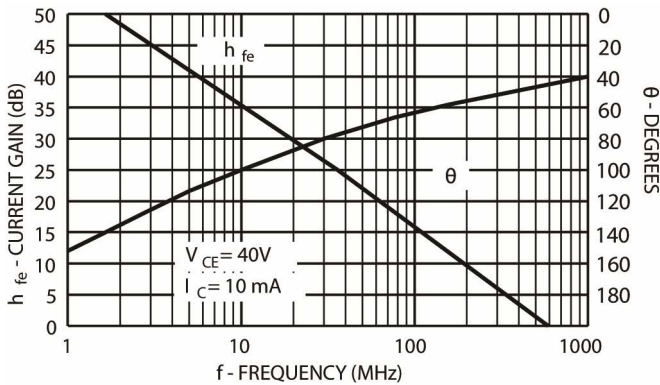


Fig 9 – Current Gain and Phase Angle versus Frequency

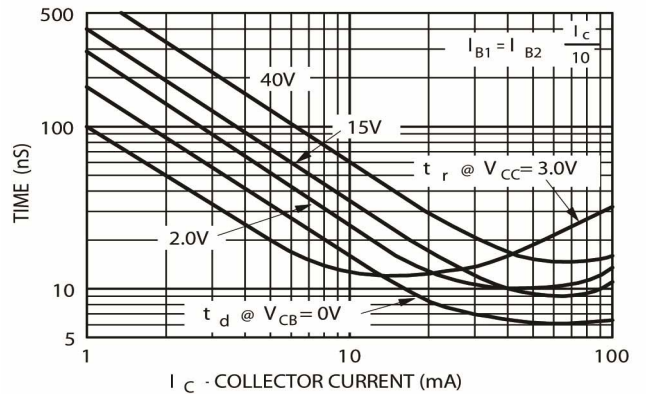


Fig 10 – Turn-On Time versus Collector Current

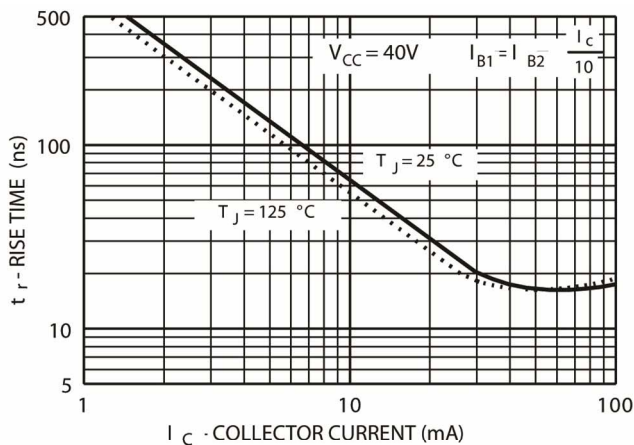


Fig 11 – Rise Time versus Collector Current

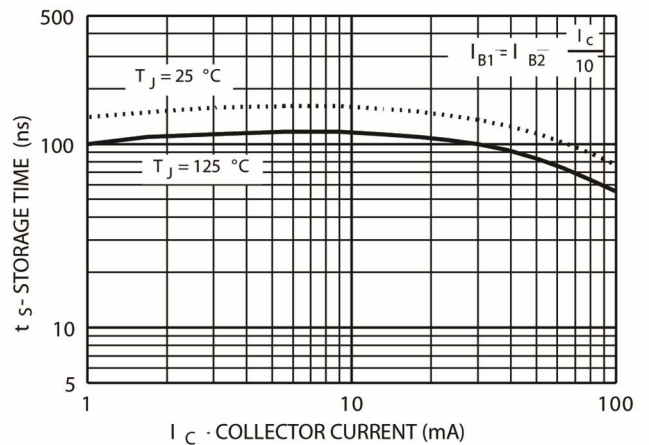


Fig 12 – Storage Time versus Collector Current





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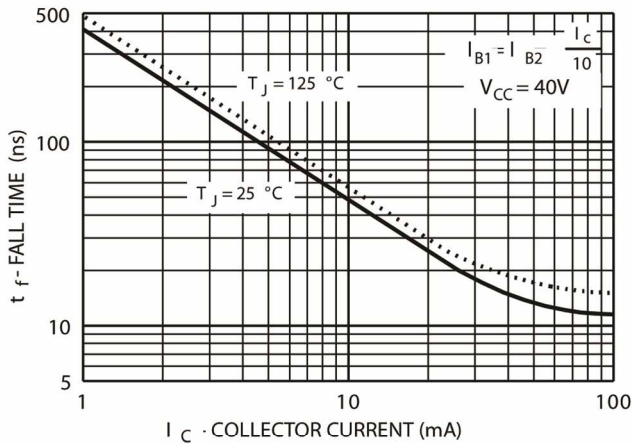


Fig 13 – Fall Time versus Collector Current

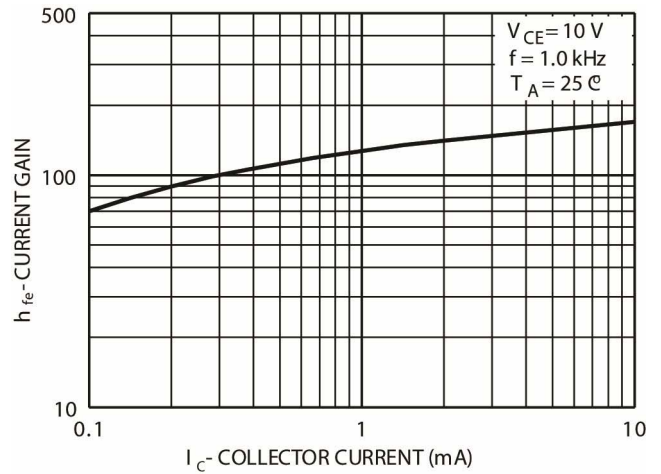


Fig 14 – Current Gain

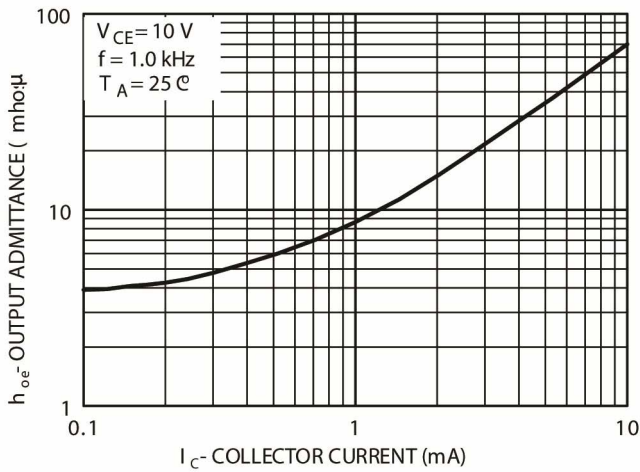


Fig 15 – Output Admittance

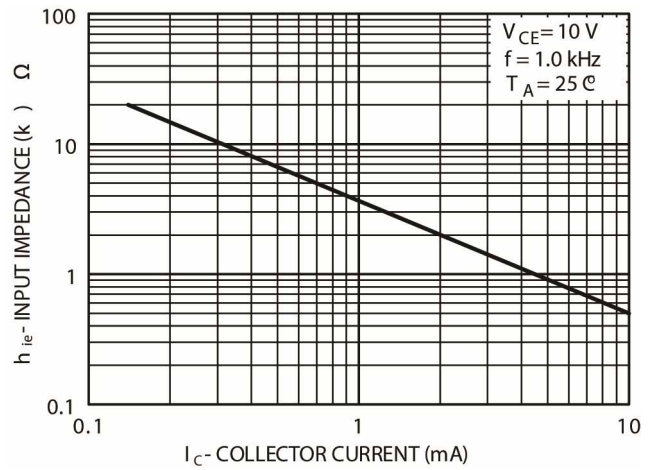


Fig 16 – Input Impedance





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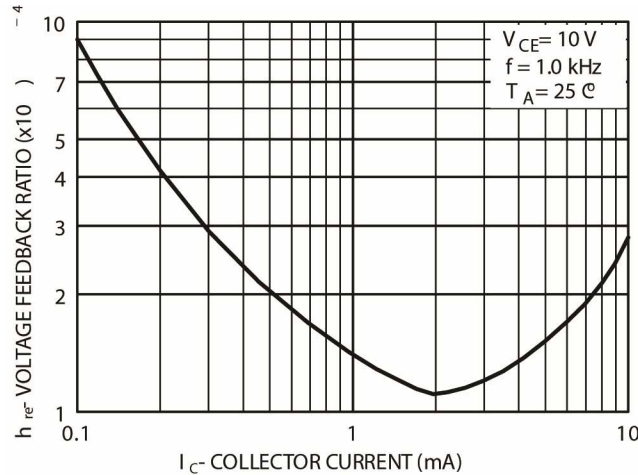


Fig 16 – Voltage Feedback Ratio

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