

4Mb Async. FAST SRAM A-die Specification

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Document Title

256Kx16 & 512Kx8 Bit Asynchronous FAST SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Mar. 2013	Preliminary
1.0	Final spec release	Jul. 2013	Final
1.1	Add wide Vcc range support 1.65 ~ 3.6V Add 48FBGA and 36FBGA PKG information	Aug. 2013	Final
1.2	Add 12ns speed binning Change ordering information table format Remove the ordering information of -UC(I)15, -XC(I)15, -NC(I)15	Nov. 2013	Final
1.3	Add 48FBGA special ball out configuration	Feb. 2015	Final

S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A 4M Async FAST SRAM

256Kx16 & 512Kx8 Bit Asynchronous FAST SRAM - Automotive

Features

- Fast Access Time : 8, 10, 12, 15ns(Max.)
- CMOS Low Power Dissipation
Standby (TTL) : 10mA (Max.)
(CMOS) : 6mA (Max.)
Operating : 35mA (8ns, Max.)
30mA (10ns, Max.)
2.4V ~ 3.6V Vcc (Automotive Temp.)
- Single 3.3±0.3V or 5.0±0.5V Power Supply
- S6R40xxV1A : 3.3 ±0.3V Power Supply
- S6R40xxC1A : 5.0 ±0.5V Power Supply
- Wide range of Power Supply
- S6R40xxW1A : 1.65V ~ 3.6V Vcc (Industrial Temp.)
- TTL Compatible Inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
LB : I/O0~ I/O7, UB : I/O8~ I/O15
- Standard 44TSOP2, 36FBGA and 48FBGA Package Pin Configuration
- Special 48FBGA Package Pin Configuration Supported
(Upper bytes and lower bytes are swapped at x16 case)
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.

General Description

The S6R4016(V/C/W)1A and S6R4008(V/C/W)1A are a 4,194,304-bit high-speed Static Random Access Memory organized as 256K (512K) words by 16(8) bits. The S6R4016(V/C/W)1A (S6R4008(V/C/W)1A) uses 16(8) common input and output lines and have an output enable pin which operates faster than address access time at read cycle. And S6R4016(V/C/W)1A allows that lower and upper byte access by data byte control(\overline{UB} , \overline{LB}). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The S6R4016(V/W)1A is packaged in a 400mil 44-pin TSOP2 and 48FBGA.

The S6R4016C1A is packaged in a 400mil 44-pin TSOP2.

The S6R4008(V/W)1A is packaged in a 400mil 44-pin TSOP2 and 36FBGA.

The S6R4008C1A is packaged in a 400mil 44-pin TSOP2.

4Mb Asynchronous FAST SRAM Ordering Information (256Kx16)

Density	Org.	Part Number	Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
4Mb	256Kx16	S6R4016V1A-UC(I)08	3.3	8	4	44 TSOP2	C : Commercial Temperature I : Industrial Temperature
		S6R4016W1A-UC(I)08	3.3	8	4	44 TSOP2	
		S6R4016W1A-UC(I)08	2.5	10	5	44 TSOP2	
		S6R4016W1A-UC(I)08	1.8	12	6	44 TSOP2	
		S6R4016V1A-XC(I)08	3.3	8	4	48 FBGA	
		S6R4016W1A-XC(I)08	3.3	8	4	48 FBGA	
		S6R4016W1A-XC(I)08	2.5	10	5	48 FBGA	
		S6R4016W1A-XC(I)08	1.8	12	6	48 FBGA	
		S6R4016C1A-UC(I)10	5.0	10	5	44 TSOP2	
		S6R4016V1A-UC(I)10	3.3	10	5	44 TSOP2	
		S6R4016W1A-UC(I)10	3.3	10	5	44 TSOP2	
		S6R4016W1A-UC(I)10	2.5	10	5	44 TSOP2	
		S6R4016W1A-UC(I)10	1.8	15	7	44 TSOP2	
		S6R4016V1A-XC(I)10	3.3	10	5	48 FBGA	
		S6R4016W1A-XC(I)10	3.3	10	5	48 FBGA	
		S6R4016W1A-XC(I)10	2.5	10	5	48 FBGA	
S6R4016W1A-XC(I)10	1.8	15	7	48 FBGA			

**S6R4016V1A, S6R4016C1A, S6R4016W1A
S6R4008V1A, S6R4008C1A, S6R4008W1A**

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4Mb Asynchronous FAST SRAM Ordering Information (256Kx16) - Special Ball Out 48FBGA

Density	Org.	Part Number	Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
4Mb	256Kx16	S6R4016WKA-XC(I)08	3.3	8	4	48 FBGA Special Ball Out Configuration	C : Commercial Temperature I : Industrial Temperature
		S6R4016WKA-XC(I)08	2.5	10	5		
		S6R4016WKA-XC(I)08	1.8	12	6		
		S6R4016WKA-XC(I)10	3.3	10	5		
		S6R4016WKA-XC(I)10	2.5	10	5		
		S6R4016WKA-XC(I)10	1.8	15	7		

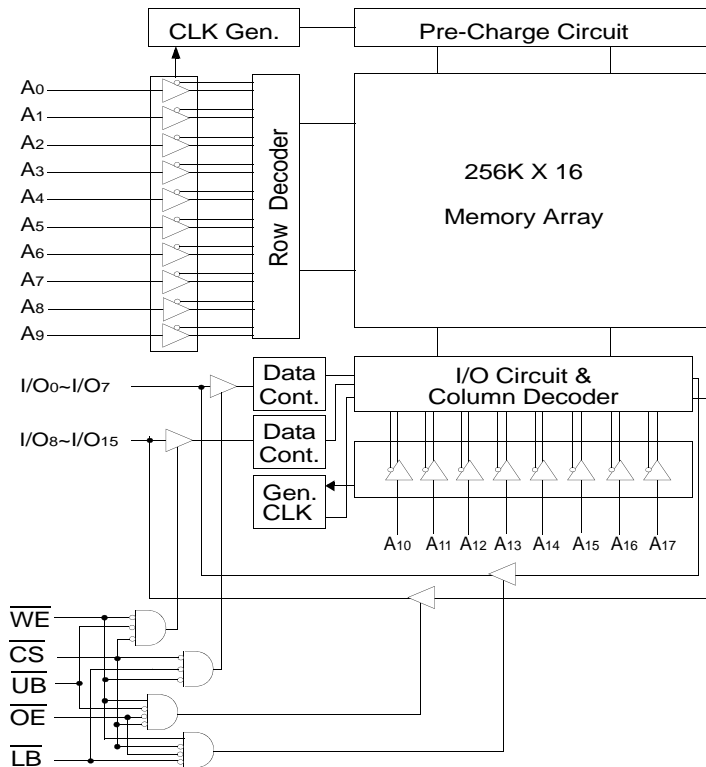
4Mb Asynchronous FAST SRAM Ordering Information (512Kx8)

Density	Org.	Part Number	Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
4Mb	512Kx8	S6R4008V1A-UC(I)08	3.3	8	4	44 TSOP2	C : Commercial Temperature I : Industrial Temperature
		S6R4008W1A-UC(I)08	3.3	8	4	44 TSOP2	
		S6R4008W1A-UC(I)08	2.5	10	5	44 TSOP2	
		S6R4008W1A-UC(I)08	1.8	12	6	44 TSOP2	
		S6R4008V1A-NC(I)08	3.3	8	4	36 FBGA	
		S6R4008W1A-NC(I)08	3.3	8	4	36 FBGA	
		S6R4008W1A-NC(I)08	2.5	10	5	36 FBGA	
		S6R4008W1A-NC(I)08	1.8	12	6	36 FBGA	
		S6R4008C1A-UC(I)10	5.0	10	5	44 TSOP2	
		S6R4008V1A-UC(I)10	3.3	10	5	44 TSOP2	
		S6R4008W1A-UC(I)10	3.3	10	5	44 TSOP2	
		S6R4008W1A-UC(I)10	2.5	10	5	44 TSOP2	
		S6R4008W1A-UC(I)10	1.8	15	7	44 TSOP2	
		S6R4008V1A-NC(I)10	3.3	10	5	36 FBGA	
		S6R4008W1A-NC(I)10	3.3	10	5	36 FBGA	
		S6R4008W1A-NC(I)10	2.5	10	5	36 FBGA	
		S6R4008W1A-NC(I)10	1.8	15	7	36 FBGA	

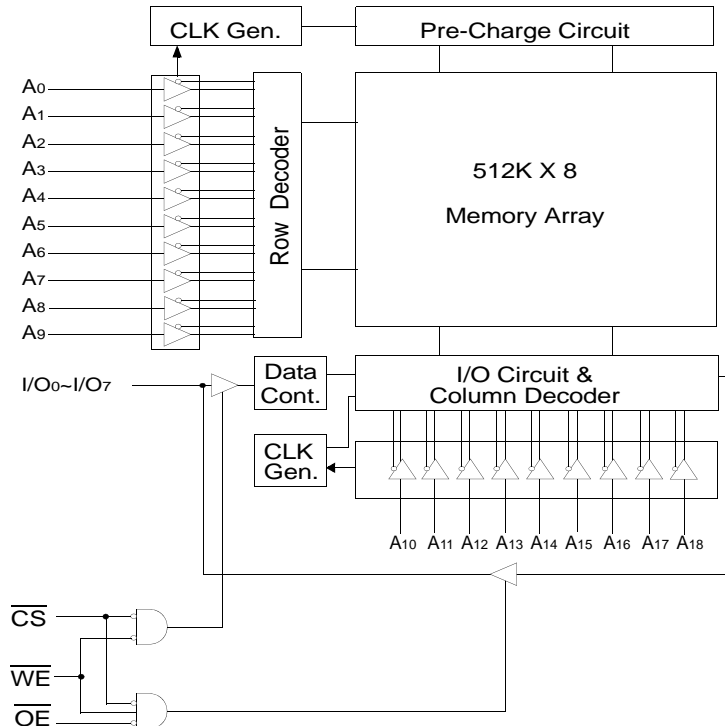
**S6R4016V1A, S6R4016C1A, S6R4016W1A
S6R4008V1A, S6R4008C1A, S6R4008W1A**

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Logic Block Diagram - S6R4016(V/C/W)1A (256K x 16)



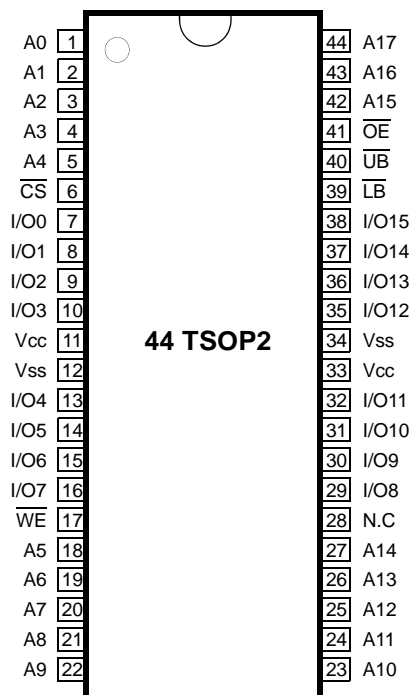
Logic Block Diagram - S6R4008(V/C/W)1A (512K x 8)



S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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44 TSOP2 Package Pin Configurations (Top View) - S6R4016(V/C/W)1A (256K x 16)



Pin Function

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
LB	Lower-byte Control(I/O0-I/O7)
UB	Upper-byte Control(I/O8-I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

48FBGA - S6R4016(V/W)1A, 256Kx16 - Top View PKG Pin Configurations

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	NC
B	I/O8	UB	A3	A4	CS	I/O0
C	I/O9	I/O10	A5	A6	I/O1	I/O2
D	Vss	I/O11	A17	A7	I/O3	Vcc
E	Vcc	I/O12	NC	A16	I/O4	Vss
F	I/O14	I/O13	A14	A15	I/O5	I/O6
G	I/O15	NC	A12	A13	WE	I/O7
H	NC	A8	A9	A10	A11	NC

Pin Function

Pin Name	Pin Function
A0 - A17	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
LB	Lower-byte Control(I/O0-I/O7)
UB	Upper-byte Control(I/O8-I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
NC	No Connection

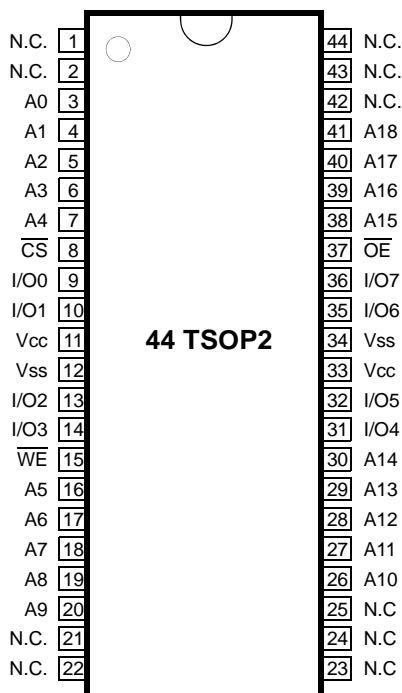
48FBGA - S6R4016WKA, 256Kx16 - Top View PKG Pin Configurations - Special Ball Out Configuration

	1	2	3	4	5	6
A	LB	OE	A0	A1	A2	NC
B	I/O0	UB	A3	A4	CS	I/O8
C	I/O1	I/O2	A5	A6	I/O10	I/O9
D	Vss	I/O3	A17	A7	I/O11	Vcc
E	Vcc	I/O4	NC	A16	I/O12	Vss
F	I/O6	I/O5	A14	A15	I/O13	I/O14
G	I/O7	NC	A12	A13	WE	I/O15
H	NC	A8	A9	A10	A11	NC

**S6R4016V1A, S6R4016C1A, S6R4016W1A
S6R4008V1A, S6R4008C1A, S6R4008W1A**

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44 TSOP2 Package Pin Configurations(Top View) - S6R4008(V/C/W)1A (512K x 8)



Pin Function

Pin Name	Pin Function
A0 - A18	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

36FBGA - S6R4008(V/W)1A, 512Kx8 - Top View

PKG Pin Configurations

	1	2	3	4	5	6
A	A ₀	A ₁	NC	A ₃	A ₆	A ₈
B	I/O ₄	A ₂	\overline{WE}	A ₄	A ₇	I/O ₀
C	I/O ₅		NC	A ₅		I/O ₁
D	Vss					Vcc
E	Vcc					Vss
F	I/O ₆		A ₁₈	A ₁₇		I/O ₂
G	I/O ₇	\overline{OE}	\overline{CS}	A ₁₆	A ₁₅	I/O ₃
H	A ₉	A ₁₀	A ₁₁	A ₁₂	A ₁₃	A ₁₄

Pin Function

Pin Name	Pin Function
A0 - A18	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground
NC	No Connection

S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to VSS	3.3V Product	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V	V
	5.0V Product			
	Wide V _{CC} ** Product			
Voltage on V _{CC} Supply Relative to VSS	3.3V Product	V _{IN} , V _{OUT}	-0.5 to 4.6	V
	5.0V Product		-0.5 to 7.0	
	Wide V _{CC} ** Product		-0.5 to 4.6	
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to +150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Wide V_{CC} range is 1.65V ~ 3.6V.

Recommended DC Operating Conditions* (T_A=0 to 70°C)

Parameter	Operating V _{CC} (V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V _{CC}	4.5	5.0	5.5	V
	3.3	V _{CC}	3.0	3.3	3.6	
	Wide 2.4 ~ 3.6	V _{CC}	2.4	2.5/3.3	3.6	
	Wide 1.65 ~ 2.2	V _{CC}	1.65	1.8	2.2	
Ground		V _{SS}	0	0	0	V
Input High Voltage	5.0	V _{IH}	2.2	-	V _{CC} +0.5	V
	3.3	V _{IH}	2.0	-	V _{CC} +0.5	
	Wide 2.4 ~ 3.6	V _{IH}	2.0	-	V _{CC} +0.3	
	Wide 1.65 ~ 2.2	V _{IH}	1.4	-	V _{CC} +0.2	
Input Low Voltage	5.0	V _{IL}	-0.3	-	0.8	V
	Wide 2.4 ~ 3.6	V _{IL}	-0.3	-	0.7	
	Wide 1.65 ~ 2.2	V _{IL}	-0.2	-	0.4	

* The above parameters are also guaranteed for industrial temperature range.

S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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DC and Operating Characteristics * (TA=0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}		-2	2	μA	
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =V _{SS} to V _{CC}		-2	2	μA	
Operating Current	I _{CC}	Min. Cycle, 100% Duty CS=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	Industrial	8ns	-	35	mA
				10ns	-	30	
				12ns	-	28	
				15ns	-	25	
Standby Current	I _{SB}	Min. Cycle, $\overline{CS}=V_{IH}$		-	10	mA	
	I _{SB1}	f=0MHz, $\overline{CS} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V		-	6		
Output Low Voltage Level	V _{OL}	V _{CC} =4.5V, I _{OL} =8mA, 5.0V Product		-	0.4	V	
		V _{CC} =3.0V, I _{OL} =8mA, 3.3V Product & Wide V _{CC} * Product		-	0.4		
		V _{CC} =2.4V, I _{OL} =1mA, Wide V _{CC} * Product		-	0.4		
		V _{CC} =1.65V, I _{OL} =0.1mA, Wide V _{CC} * Product		-	0.2		
Output High Voltage Level	V _{OH}	V _{CC} =4.5V, I _{OH} =-4mA, 5.0V Product		2.4	-	V	
		V _{CC} =3.0V, I _{OH} =-4mA, 3.3V Product & Wide V _{CC} * Product		2.4	-		
		V _{CC} =2.4V, I _{OH} =-1mA, Wide V _{CC} * Product		1.8	-		
		V _{CC} =1.65V, I _{OH} =-0.1mA, Wide V _{CC} * Product		1.4	-		

* The above parameters are also guaranteed for industrial temperature range.

** Wide V_{CC} range is 1.65V ~ 3.6V.

Capacitance* (TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

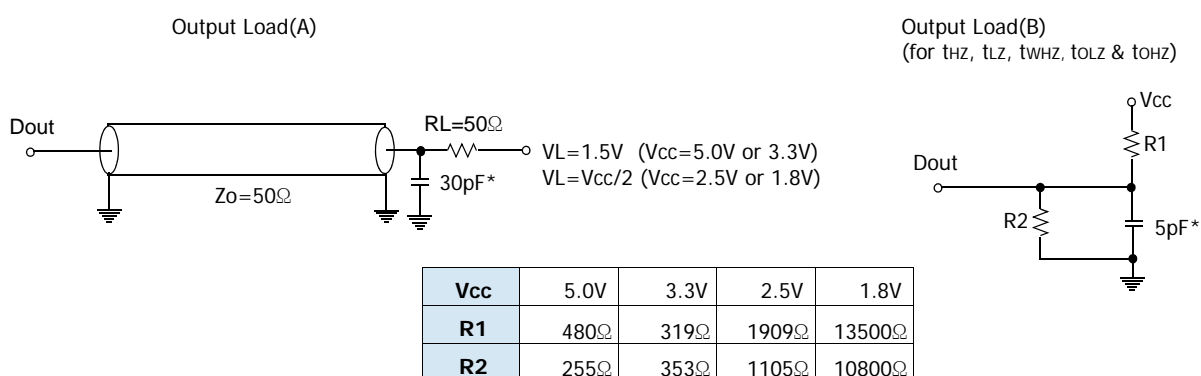
* Capacitance is sampled and not 100% tested.

S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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Test Conditions

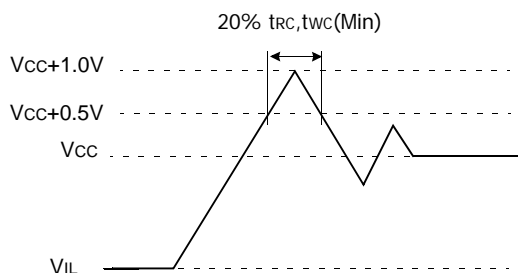
Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V or 5.0V)
	0 to 2.5V (Vcc=2.5V)
	0 to 1.8V (Vcc=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V or 5.0V)
	1/2Vcc (Vcc=1.8V or 2.5V)
Output Load	See Fig. 1



* Including Scope and Jig Capacitance

Fig. 1

Overshoot Timing



Undershoot Timing

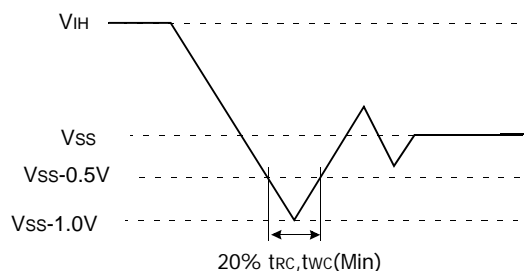


Fig. 2

Functional Description (x8 Mode)

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	ISB, ISB1
L	H	H	Output Disable	High-Z	Icc
L	H	L	Read	DOUT	Icc
L	L	X	Write	DIN	Icc

* X means Don't Care.

S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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Functional Description (x16 Mode)

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}^{**}	\overline{UB}^{**}	Mode	I/O Pin		Supply Current
						I/O ₀ ~I/O ₇	I/O ₈ ~I/O ₁₅	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	I _{CC}
L	X	X	H	H				
L	H	L	L	H	Read	DOUT	High-Z	I _{CC}
			H	L		High-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	I _{CC}
			H	L		High-Z	DIN	
			L	L		DIN	DIN	

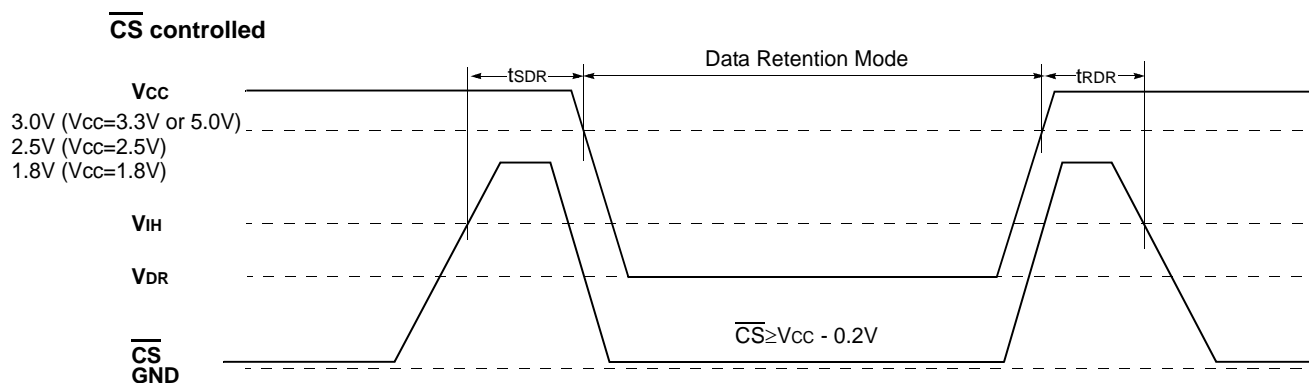
* X means Don't Care.

Data Retention Characteristics* (TA=0 to 70°C)

Parameter	Product	Operating V _{CC} (V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V _{CC} for Data Retention	5.0V Product	5.0	V _D R	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	5.5	V
	3.3V Product	3.3			2.0	-	3.6	
	Wide 2.4V ~ 3.6V	2.5/3.3			2.0	-	3.6	
	Wide 1.65V ~ 2.2V	1.8			1.5	-	3.6	
Data Retention Current	5.0V Product	5.0	I _D R	V _{CC} =2.0V $\overline{CS} \geq V_{CC} - 0.2V$ V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	-	-	5	mA
	3.3V Product	3.3			-	-	5	
	Wide 2.4V ~ 3.6V	2.5/3.3			-	-	6	
	Wide 1.65V ~ 2.2V	1.8			-	-	6	
Data Retention Set-Up Time			t _{SDR}	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time			t _{RDR}		5	-	-	ms

* The above parameters are also guaranteed for industrial temperature range.

Data Retention Wave Form



S6R4016V1A, S6R4016C1A, S6R4016W1A S6R4008V1A, S6R4008C1A, S6R4008W1A

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Read Cycle*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	8	-	10	-	12	-	15	-	ns
Address Access Time	tAA	-	8	-	10	-	12	-	15	ns
Chip Select to Output	tCO	-	8	-	10	-	12	-	15	ns
Output Enable to Valid Output	tOE	-	4	-	5	-	6	-	7	ns
\overline{UB} , \overline{LB} Access Time *	tBA	-	4	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	tLZ	3	-	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	tOLZ	0	-	0	-	0	-	0	-	ns
\overline{UB} , \overline{LB} Enable to Low-Z Output *	tBLZ	0	-	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	tHZ	0	4	0	5	0	6	0	7	ns
Output Disable to High-Z Output	tOHZ	0	4	0	5	0	6	0	7	ns
\overline{UB} , \overline{LB} Disable to High-Z Output *	tBHZ	0	4	0	5	0	6	0	7	ns
Output Hold from Address Change	tOH	3	-	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	tPU	0	-	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	tPD	-	8	-	10	-	12	-	15	ns

* The above parameters are also guaranteed for industrial temperature range.

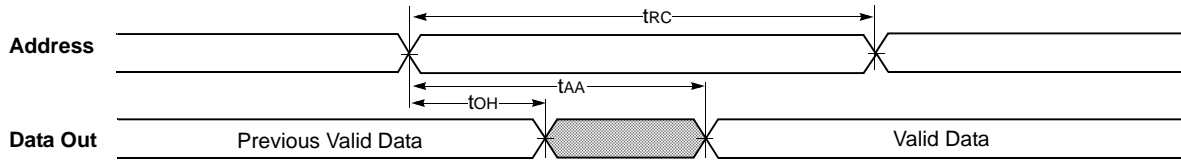
Write Cycle*

Parameter	Symbol	8ns		10ns		12ns		15ns		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	8	-	10	-	12	-	15	-	ns
Chip Select to End of Write	tCW	6	-	7	-	9	-	12	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	0	-	ns
Address Valid to End of Write	tAW	6	-	7	-	9	-	12	-	ns
Write Pulse Width(\overline{OE} High)	tWP	6	-	7	-	9	-	12	-	ns
Write Pulse Width(\overline{OE} Low)	tWP1	8	-	10	-	12	-	15	-	ns
\overline{UB} , \overline{LB} Valid to End of Write *	tBW	6	-	7	-	9	-	12	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	4	0	5	0	6	0	7	ns
Data to Write Time Overlap	tDW	4	-	5	-	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	0	-	0	-	ns
End of Write to Output Low-Z	tOW	3	-	3	-	3	-	3	-	ns

* The above parameters are also guaranteed for industrial temperature range.

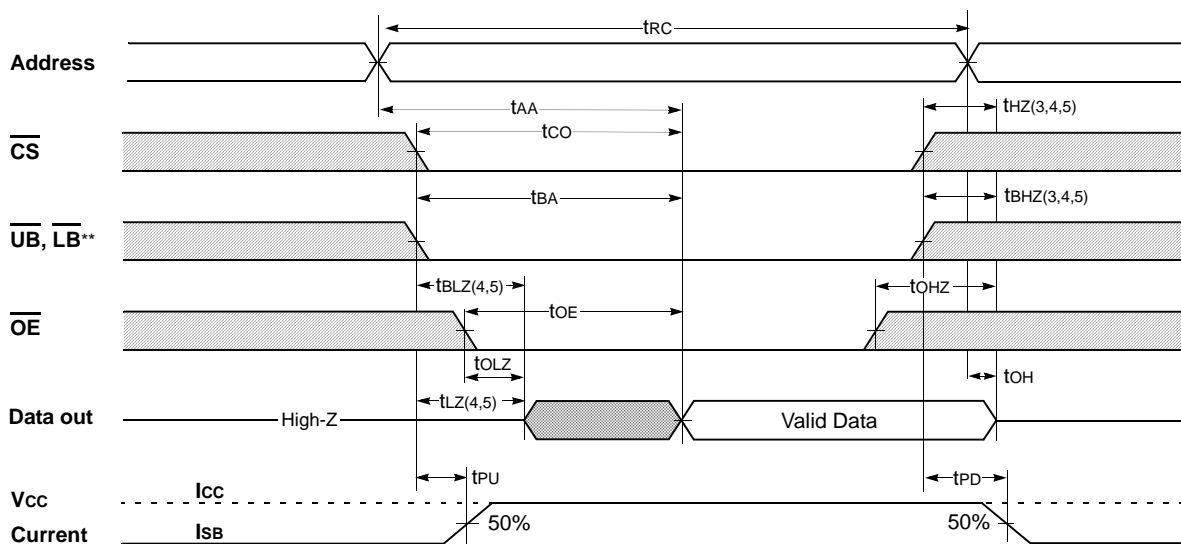
Timing Diagrams

Timing Waveform Of Read Cycle(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, $\overline{UB}, \overline{LB}=V_{IL}$ **)



** Those parameters are applied for x16 mode only.

Timing Waveform Of Read Cycle(2) ($\overline{WE}=V_{IH}$)

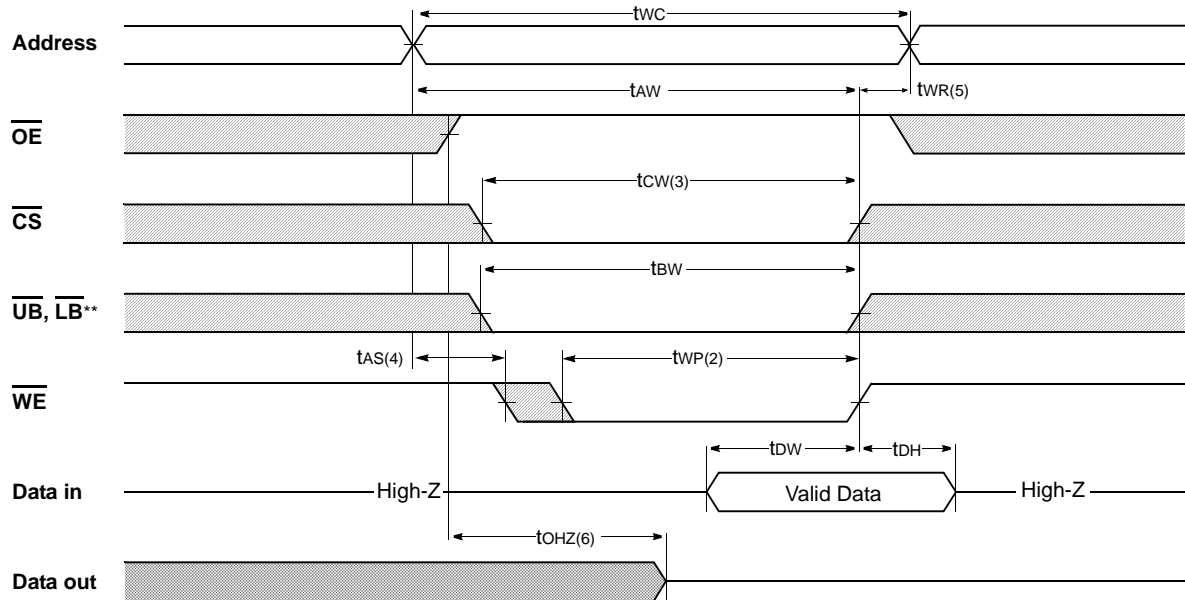


NOTES(Read Cycle)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

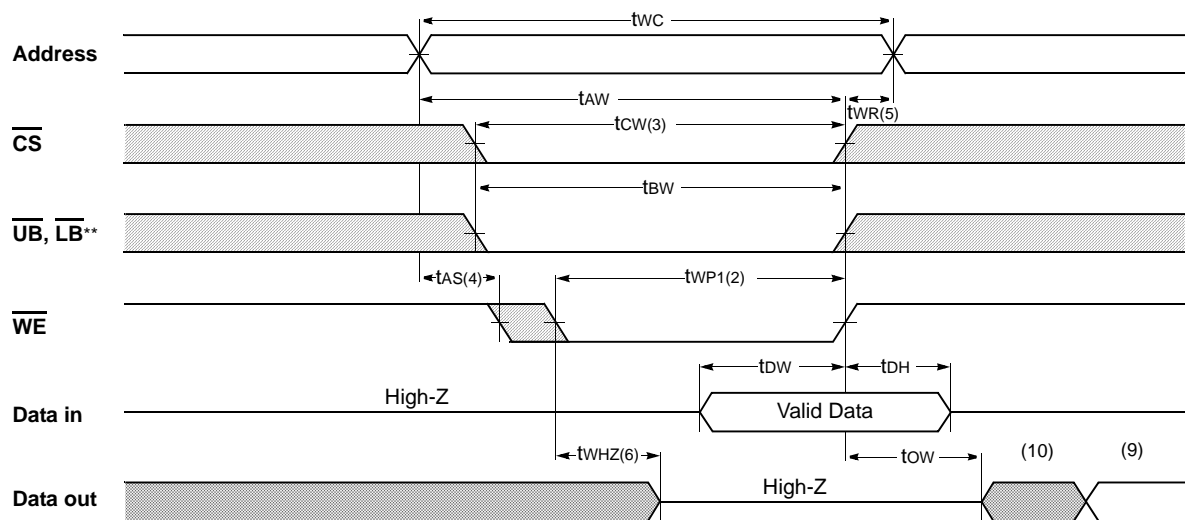
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(1) (\overline{OE} Clock)



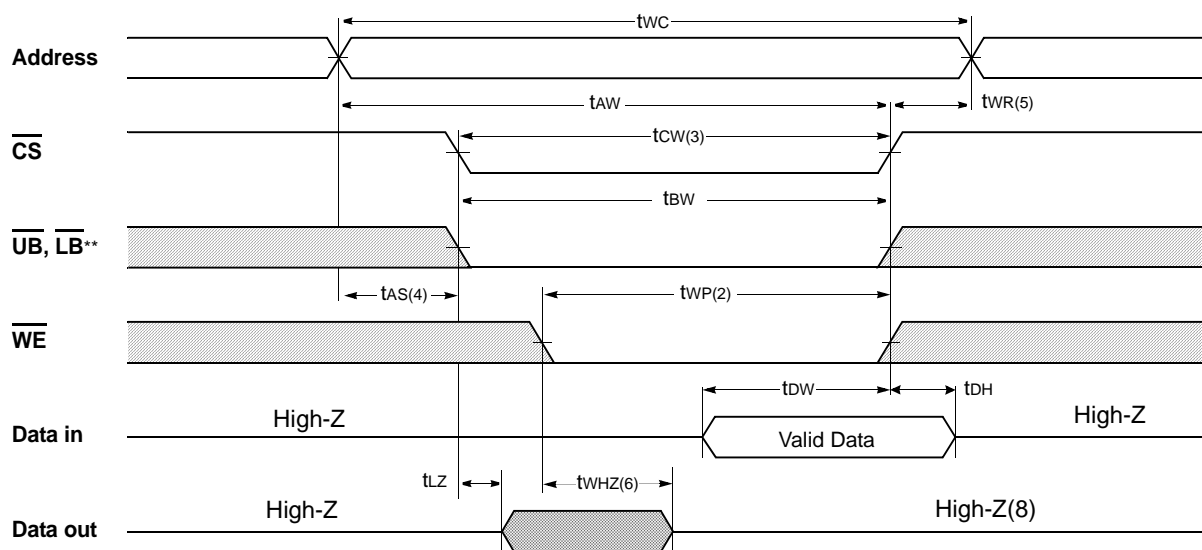
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) (\overline{OE} =Low fixed)



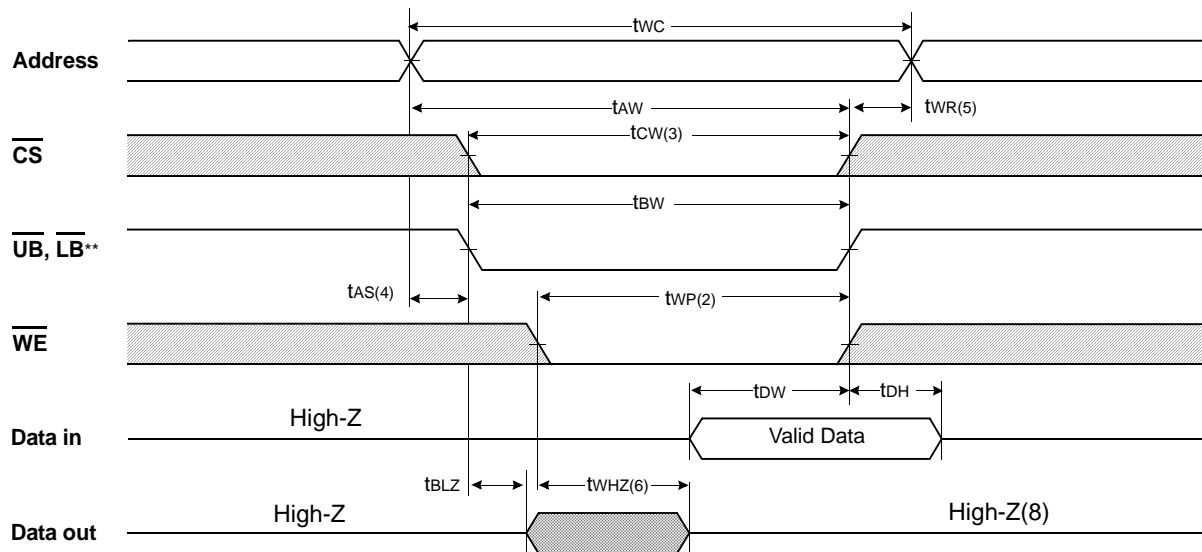
** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(3) (\overline{CS} =Controlled)



** Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(4) (\overline{UB} , \overline{LB} Controlled)



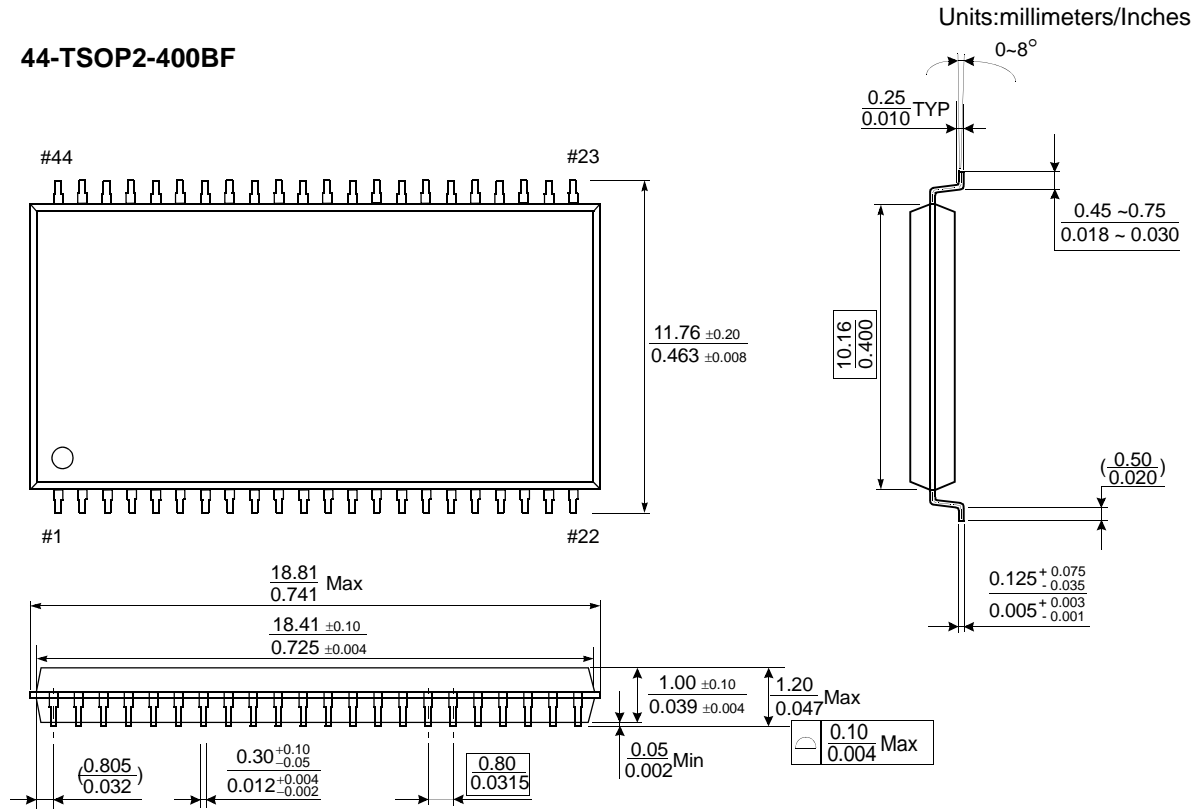
NOTES(Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low \overline{CS} , \overline{WE} , \overline{LB} and \overline{UB} . A write begins at the latest transition \overline{CS} going low and \overline{WE} going low ; A write ends at the earliest transition \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of \overline{CS} going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.
6. If \overline{OE} , \overline{CS} and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not . be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If \overline{CS} goes low simultaneously with \overline{WE} going or after \overline{WE} going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When \overline{CS} is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

** Those parameters are applied for x16 mode only.

Package Dimensions

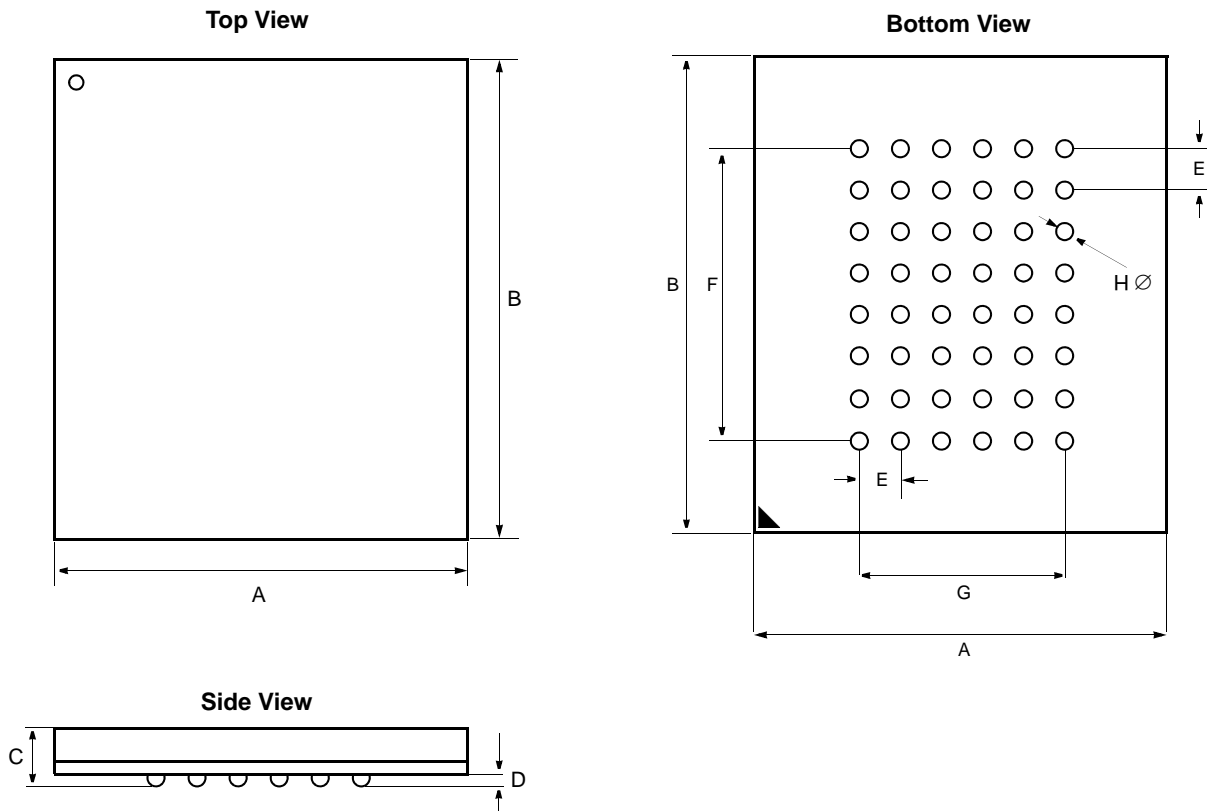
44-TSOP2-400BF



Package Dimensions

48-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array

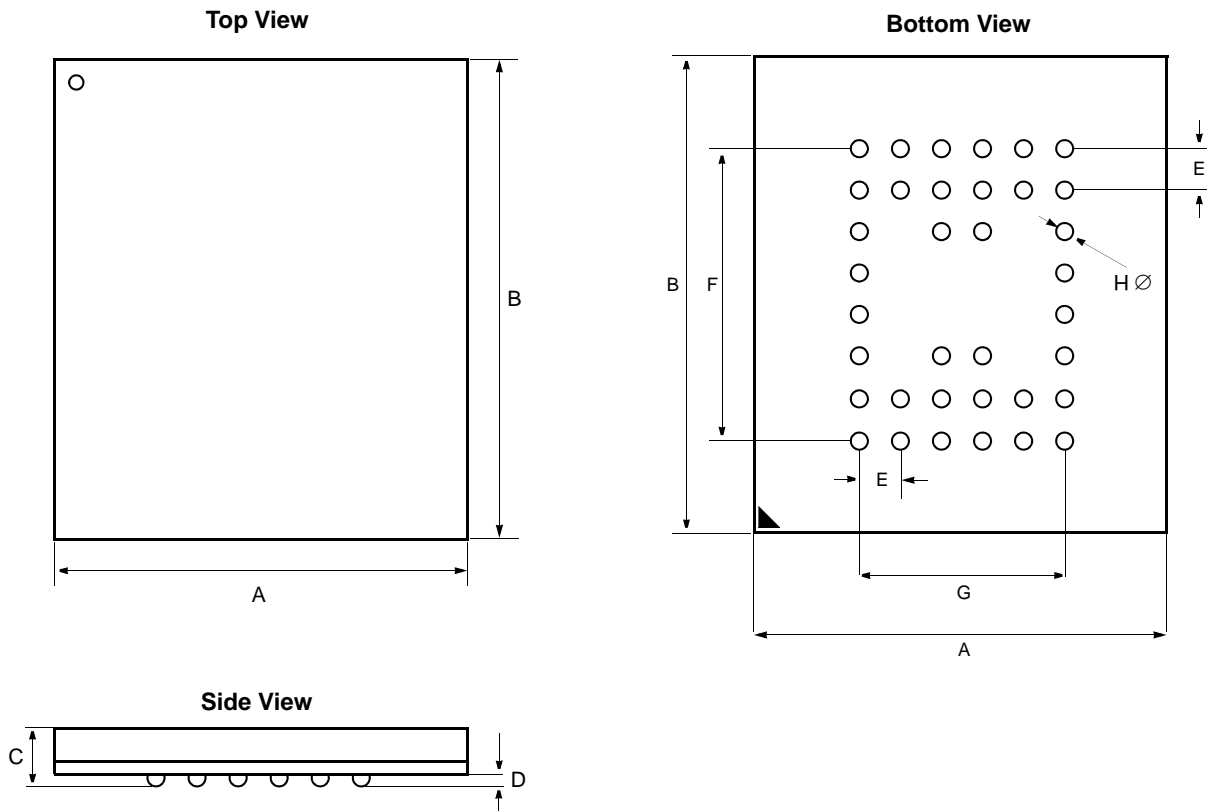


Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	6 ± 0.1	mm		E	0.75	mm	
B	8 ± 0.1	mm		F	5.25	mm	
C	1.1 ± 0.1	mm		G	3.75	mm	
D	0.25 ± 0.05	mm		H	0.35 ± 0.05	mm	

Package Dimensions

36-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	6 ± 0.1	mm		E	0.75	mm	
B	8 ± 0.1	mm		F	5.25	mm	
C	1.1 ± 0.1	mm		G	3.75	mm	
D	0.25 ± 0.05	mm		H	0.35 ± 0.05	mm	