

1Mb Low Power SRAM M-die Specification

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Document Title

64Kx16 & 128Kx8 Bit Low Power SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial Draft	Nov. 2015	Preliminary
0.1	Add typical I _{DR} value	Dec. 2015	Preliminary
1.0	Final version release Split I _{CC1} spec value depending on V _{CC} ; 2.3~3.6V : 3mA ; 4.5~5.5V : 4mA Add 32SOP and 32TSOP2	Feb. 2016	Final
1.1	Add commercial temperature range	Apr. 2016	Final

S6L1016W, S6L1016C S6L1008W, S6L1008C

1M Low Power SRAM

64Kx16 & 128Kx8 Bit Low Power SRAM

Features

- Fast Access Time : 45, 55, 70ns(Max.)
- CMOS Low Power Dissipation
Standby Current (Typical) : 2 μ A
(Maximum) : 10 μ A
Operating Current (Typical) : 15mA (tAA=55ns)
(Maximum) : 20mA (tAA=55ns)
- Wide range or Single 5.0V Power Supply
- S6L10xxW : 2.3V ~ 3.6V Vcc
- S6L10xxC : 4.5V ~ 5.5V Vcc
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control (x16 Mode)
LB : I/O0~ I/O7, UB : I/O8~ I/O15
- Standard 32SOP, 32TSOP1, 32sTSOP1, 32TSOP2,
44TSOP2, 48FBGA Package Pin Configuration
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.
- 2CS Option Available

General Description

The S6L1016(W/C) and S6L1008(W/C) are a 1,048,576-bit high-speed Static Random Access Memory organized as 64K (128K) words by 16(8) bits. S6L1016(W/C) allows that lower and upper byte access by data byte control(\overline{UB} , \overline{LB}). The device is fabricated using advanced CMOS process, 6-TR based cell technology and designed for low power circuit technology. It is particularly well suited for use in battery back up application for low data retention current.

The S6L1016(W/C) is packaged in a 44TSOP2 and 48FBGA. The S6L1008(W/C) is packaged in a 32SOP, 32TSOP1, 32sTSOP1 and 32TSOP2.

1Mb Low Power SRAM Ordering Information (64Kx16) - 1CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	64Kx16	S6L1016W1M-UC(I)45	2.5, 3.3	45	20	44 TSOP2	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1016W1M-UC(I)55	2.5, 3.3	55	25	44 TSOP2	
		S6L1016W1M-UC(I)70	2.5, 3.3	70	35	44 TSOP2	
		S6L1016C1M-UC(I)45	5.0	45	20	44 TSOP2	
		S6L1016C1M-UC(I)55	5.0	55	25	44 TSOP2	
		S6L1016C1M-UC(I)70	5.0	70	35	44 TSOP2	
		S6L1016W1M-XC(I)45	2.5, 3.3	45	20	48 FBGA	
		S6L1016W1M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L1016W1M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L1016C1M-XC(I)45	5.0	45	20	48 FBGA	
		S6L1016C1M-XC(I)55	5.0	55	25	48 FBGA	
		S6L1016C1M-XC(I)70	5.0	70	35	48 FBGA	

S6L1016W, S6L1016C
S6L1008W, S6L1008C

1M Low Power SRAM

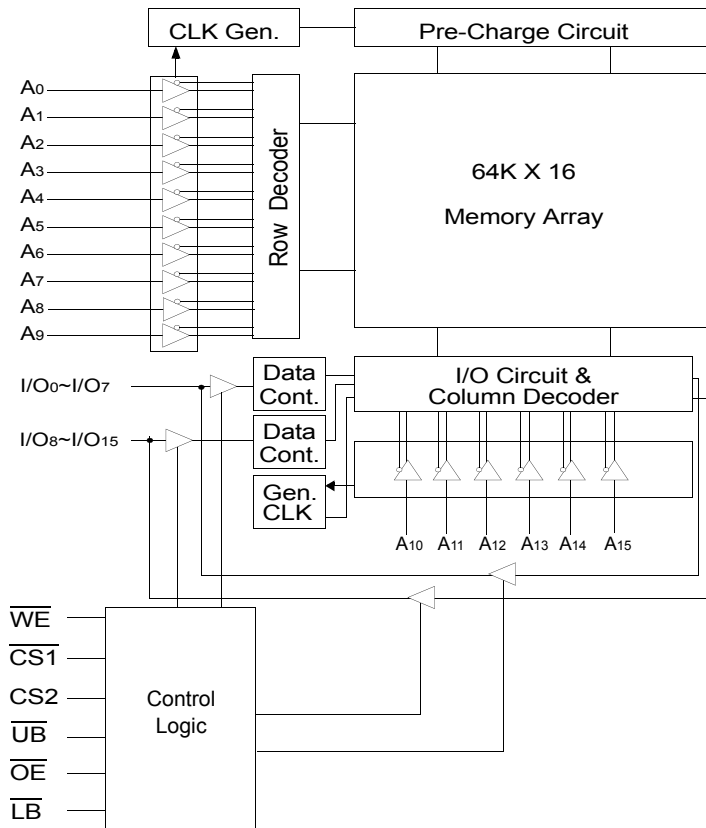
1Mb Low Power SRAM Ordering Information (64Kx16) - 2CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	64Kx16	S6L1016W2M-XC(I)45	2.5, 3.3	45	20	48 FBGA	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1016W2M-XC(I)55	2.5, 3.3	55	25	48 FBGA	
		S6L1016W2M-XC(I)70	2.5, 3.3	70	35	48 FBGA	
		S6L1016C2M-XC(I)45	5.0	45	20	48 FBGA	
		S6L1016C2M-XC(I)55	5.0	55	25	48 FBGA	
		S6L1016C2M-XC(I)70	5.0	70	35	48 FBGA	

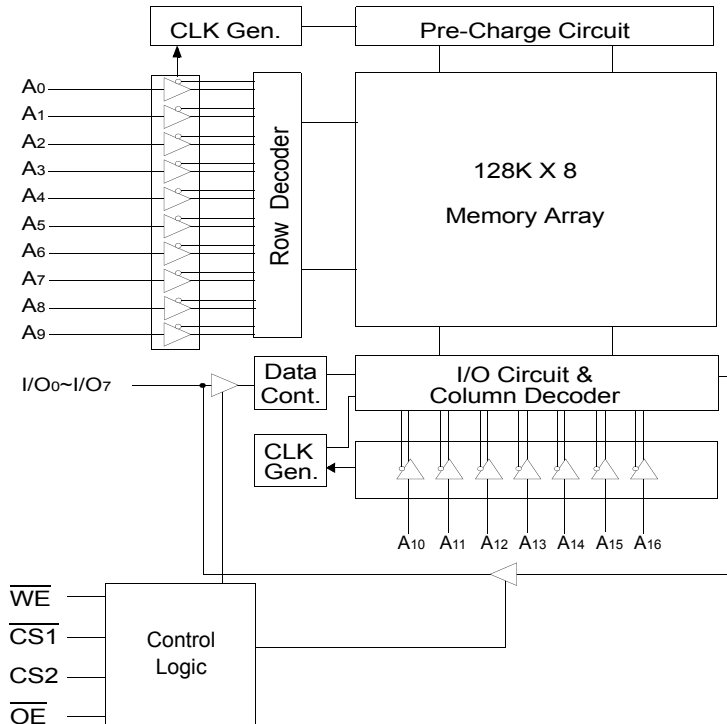
1Mb Low Power SRAM Ordering Information (128Kx8) - 2CS

Density	Org.	Part Number	Typical Vcc (V)	Speed		Package	TEMP
				tAA(ns)	tOE(ns)		
1Mb	128Kx8	S6L1008W2M-BC(I)45	2.5, 3.3	45	20	32 SOP	C : Commercial Temp. (0°C ~ 70°C) I : Industrial Temp. (-40°C ~ 85°C)
		S6L1008W2M-BC(I)55	2.5, 3.3	55	25	32 SOP	
		S6L1008W2M-BC(I)70	2.5, 3.3	70	35	32 SOP	
		S6L1008C2M-BC(I)45	5.0	45	20	32 SOP	
		S6L1008C2M-BC(I)55	5.0	55	25	32 SOP	
		S6L1008C2M-BC(I)70	5.0	70	35	32 SOP	
		S6L1008W2M-TC(I)45	2.5, 3.3	45	20	32 TSOP1	
		S6L1008W2M-TC(I)55	2.5, 3.3	55	25	32 TSOP1	
		S6L1008W2M-TC(I)70	2.5, 3.3	70	35	32 TSOP1	
		S6L1008C2M-TC(I)45	5.0	45	20	32 TSOP1	
		S6L1008C2M-TC(I)55	5.0	55	25	32 TSOP1	
		S6L1008C2M-TC(I)70	5.0	70	35	32 TSOP1	
		S6L1008W2M-LC(I)45	2.5, 3.3	45	20	32 sTSOP1	
		S6L1008W2M-LC(I)55	2.5, 3.3	55	25	32 sTSOP1	
		S6L1008W2M-LC(I)70	2.5, 3.3	70	35	32 sTSOP1	
		S6L1008C2M-LC(I)45	5.0	45	20	32 sTSOP1	
		S6L1008C2M-LC(I)55	5.0	55	25	32 sTSOP1	
		S6L1008C2M-LC(I)70	5.0	70	35	32 sTSOP1	
		S6L1008W2M-NC(I)45	2.5, 3.3	45	20	32TSOP2	
		S6L1008W2M-NC(I)55	2.5, 3.3	55	25	32TSOP2	
		S6L1008W2M-NC(I)70	2.5, 3.3	70	35	32TSOP2	
		S6L1008C2M-NC(I)45	5.0	45	20	32TSOP2	
		S6L1008C2M-NC(I)55	5.0	55	25	32TSOP2	
		S6L1008C2M-NC(I)70	5.0	70	35	32TSOP2	

Logic Block Diagram - 64K x 16



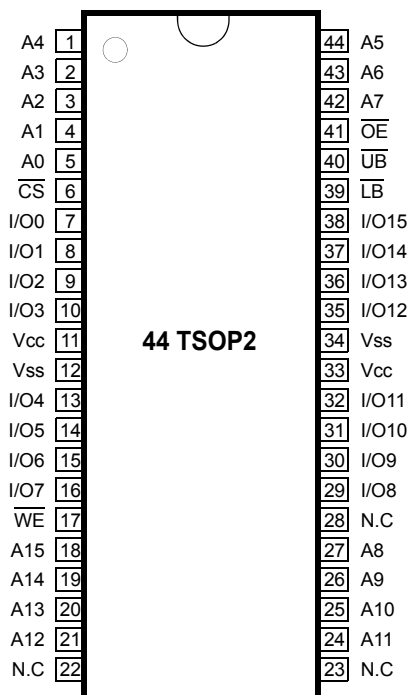
Logic Block Diagram - 128K x 8



**S6L1016W, S6L1016C
S6L1008W, S6L1008C**

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44 TSOP2 Package Pin Configurations (Top View) - S6L1016(W/C)1M (64K x 16) - 1CS

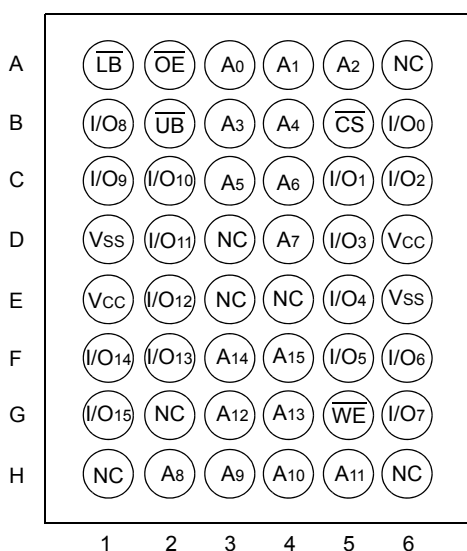


Pin Function

Pin Name	Pin Function
A0 - A15	Address Inputs
\overline{WE}	Write Enable Input
\overline{CS}	Chip Select Input
\overline{OE}	Output Enable Input
\overline{LB}	Lower-byte Control(I/O0~I/O7)
\overline{UB}	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

48FBGA - S6L1016(W/C)1M (64K x 16) - 1CS - Top View

PKG Pin Configurations



Pin Function

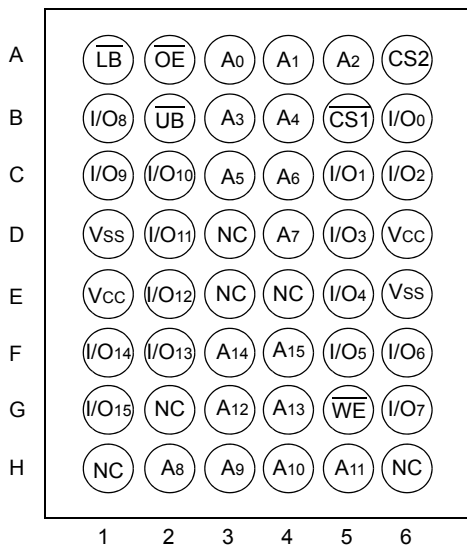
Pin Name	Pin Function
A0 - A15	Address Inputs
\overline{WE}	Write Enable Input
\overline{CS}	Chip Select Input
\overline{OE}	Output Enable Input
\overline{LB}	Lower-byte Control(I/O0~I/O7)
\overline{UB}	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

**S6L1016W, S6L1016C
S6L1008W, S6L1008C**

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48FBGA - S6L1016(W/C)2M (64K x 16) - 2CS - Top View

PKG Pin Configurations

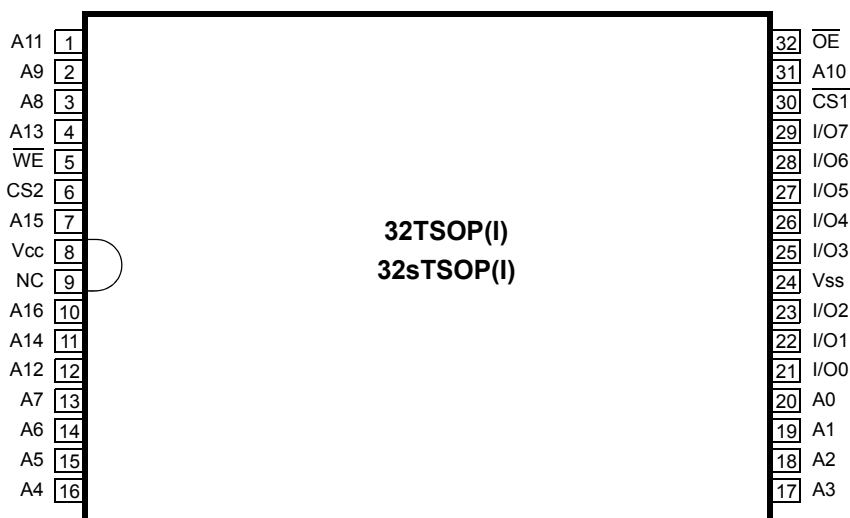


Pin Function

Pin Name	Pin Function
A0 - A15	Address Inputs
WE	Write Enable Input
CS1	Chip Select Input1
CS2	Chip Select Input2
OE	Output Enable Input
LB	Lower-byte Control(I/O0~I/O7)
UB	Upper-byte Control(I/O8~I/O15)
I/O0 ~ I/O15	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

32 TSOP1 and 32 sTSOP1 Package(Top View) - S6L1008(W/C)2M (512K x 8) - 2CS

PKG Pin Configurations

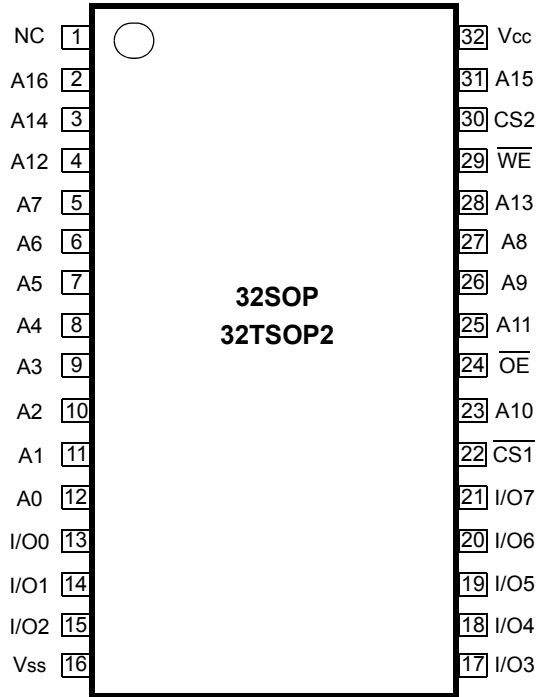


Pin Function

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS1	Chip Select1
CS2	Chip Select2
OE	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground

32 SOP and 32 TSOP2 Package(Top View) - S6L1008(W/C)2M (512K x 8) - 2CS

PKG Pin Configurations



Pin Function

Pin Name	Pin Function
A0 - A16	Address Inputs
WE	Write Enable
CS1	Chip Select1
CS2	Chip Select2
OE	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
Vcc	Power
Vss	Ground

S6L1016W, S6L1016C
S6L1008W, S6L1008C

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Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin relative to Vss		V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5V	V
Voltage on Vcc Supply Relative to Vss	Wide Vcc** Product	V _{IN} , V _{OUT}	-0.5 to 4.6	V
	5.0V Product		-0.5 to 7.0	
Power Dissipation		P _D	1.0	W
Storage Temperature		T _{STG}	-65 to +150	°C
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Wide Vcc range is 2.3V ~ 3.6V.

Recommended DC Operating Conditions (TA= -40 to 85°C)

Parameter	Operating Vcc(V)	Symbol	Min	Typ	Max	Unit
Supply Voltage	5.0	V _{CC}	4.5	5.0	5.5	V
	Wide 2.3 ~ 3.6	V _{CC}	2.3	2.5/3.3	3.6	
Ground		V _{SS}	0	0	0	V
Input High Voltage	5.0	V _{IH}	2.2	-	V _{CC} +0.5	V
	Wide 2.3 ~ 2.7	V _{IH}	1.8	-	V _{CC} +0.3	
	Wide 2.7 ~ 3.6	V _{IH}	2.2	-	V _{CC} +0.3	
Input Low Voltage	5.0	V _{IL}	-0.3	-	0.8	V
	Wide 2.3 ~ 2.7	V _{IL}	-0.3	-	0.6	
	Wide 2.7 ~ 3.6	V _{IL}	-0.3	-	0.8	

S6L1016W, S6L1016C
S6L1008W, S6L1008C

1M Low Power SRAM

DC and Operating Characteristics (TA= -40 to 85°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output Leakage Current	I _{LO}	$\overline{CS1}=V_{IH}$ or $\overline{CS2}=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$	-1	-	1	μA	
Operating Current	I _{CC}	f=f _{max} , V _{CC} =V _{CCmax} , I _{OUT} =0mA, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	45ns	-	-	20	mA
			55ns	-	-	20	
			70ns	-	-	15	
	I _{CC1}	f=1MHz, V _{CC} =V _{CCmax} , I _{OUT} =0mA, V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V	V _{CC} =2.3~3.6V		-	-	3
V _{CC} =4.5~5.5V		-	-	4			
Standby Current	I _{SB} (TTL)	V _{CC} =V _{CCmax} , CS2=V _{IL} , Others=V _{IH} or V _{IL}	2CS	-	-	0.3	mA
		V _{CC} =V _{CCmax} , $\overline{CS1}=V_{IH}$, Others=V _{IH} or V _{IL}	1CS	-	-	0.3	
	I _{SB1} (CMOS)	V _{CC} =V _{CCmax} , V _{IN} ≥V _{CC} -0.2V or V _{IN} ≤0.2V, 1) CS2≤0.2V, or 2) CS2≥V _{CC} -0.2V, $\overline{CS1} \geq V_{CC}-0.2V$, or 3) CS2≥V _{CC} -0.2V, CS1≤0.2V, UB=LB≥V _{CC} -0.2V	2CS	-	2	10	μA
			1CS	-	-	-	
Output Low Voltage Level	V _{OL}	V _{CC} =4.5V, I _{OL} =2.1mA, 5.0V Product	-	-	0.4	V	
		V _{CC} =2.7V, I _{OL} =2.1mA, Wide V _{CC} * Product	-	-	0.4		
		V _{CC} =2.3V, I _{OL} =2.1mA, Wide V _{CC} * Product	-	-	0.4		
Output High Voltage Level	V _{OH}	V _{CC} =4.5V, I _{OH} =-1mA, 5.0V Product	2.4	-	-	V	
		V _{CC} =2.7V, I _{OH} =-1mA, Wide V _{CC} * Product	2.4	-	-		
		V _{CC} =2.3V, I _{OH} =-1mA, Wide V _{CC} * Product	1.8	-	-		

Note : Typical parameters indicates the value for the center of distribution at V_{CC}=3.0V and Ta=25°C, and not 100% tested.

* Wide V_{CC} range is 2.3V ~ 3.6V.

Capacitance*(TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	TYP	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* Capacitance is sampled and not 100% tested.

S6L1016W, S6L1016C
S6L1008W, S6L1008C

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Functional Description (x8 Mode) - 2CS

$\overline{CS1}$	CS2	\overline{WE}	\overline{OE}	Mode	I/O Pin	Supply Current
H	X*	X	X	Not Select	High-Z	ISB, ISB1
X	L	X	X	Not Select	High-Z	ISB, ISB1
L	H	H	H	Output Disable	High-Z	Icc
L	H	H	L	Read	DOUT	Icc
L	H	L	X	Write	DIN	Icc

* X means Don't Care.

Functional Description (x16 Mode) - 1CS

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	I/O Pin		Mode	Supply Current
					I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅		
H	X*	X	X	X	High-Z	High-Z	Not Select	ISB, ISB1
X	X	X	H	H	High-Z	High-Z	Not Select	ISB, ISB1
L	H	H	L	X	High-Z	High-Z	Output disable	Icc
L	H	H	X	L	High-Z	High-Z	Output disable	Icc
L	H	L	L	H	DOUT	High-Z	Lower Byte Read	Icc
			H	L	High-Z	DOUT	Upper Byte Read	
			L	L	DOUT	DOUT	Word Read	
L	L	X	L	H	DIN	High-Z	Lower Byte Write	Icc
			H	L	High-Z	DIN	Upper Byte Write	
			L	L	DIN	DIN	Word Write	

* X means Don't Care.

Functional Description (x16 Mode) - 2CS

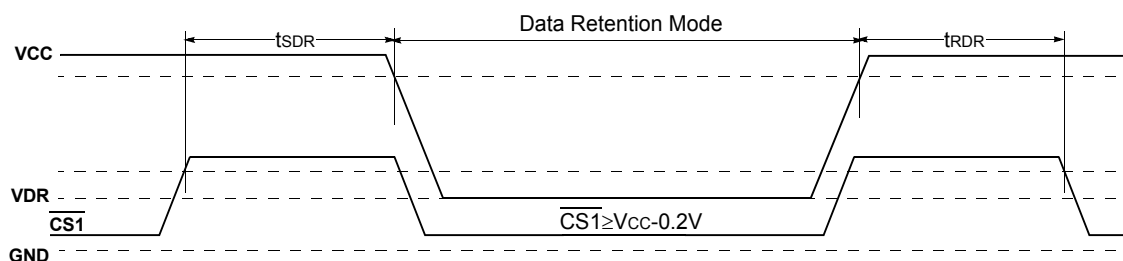
$\overline{CS1}$	CS2	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	I/O Pin		Mode	Supply Current
						I/O ₀ -I/O ₇	I/O ₈ -I/O ₁₅		
H	X*	X	X	X	X	High-Z	High-Z	Not Select	ISB, ISB1
X	L	X	X	X	X	High-Z	High-Z	Not Select	ISB, ISB1
X	X	X	X	H	H	High-Z	High-Z	Not Select	ISB, ISB1
L	H	H	H	L	X	High-Z	High-Z	Output disable	Icc
L	H	H	H	X	L	High-Z	High-Z	Output disable	Icc
L	H	H	L	L	H	DOUT	High-Z	Lower Byte Read	Icc
				H	L	High-Z	DOUT	Upper Byte Read	
				L	L	DOUT	DOUT	Word Read	
L	H	L	X	L	H	DIN	High-Z	Lower Byte Write	Icc
				H	L	High-Z	DIN	Upper Byte Write	
				L	L	DIN	DIN	Word Write	

* X means Don't Care.

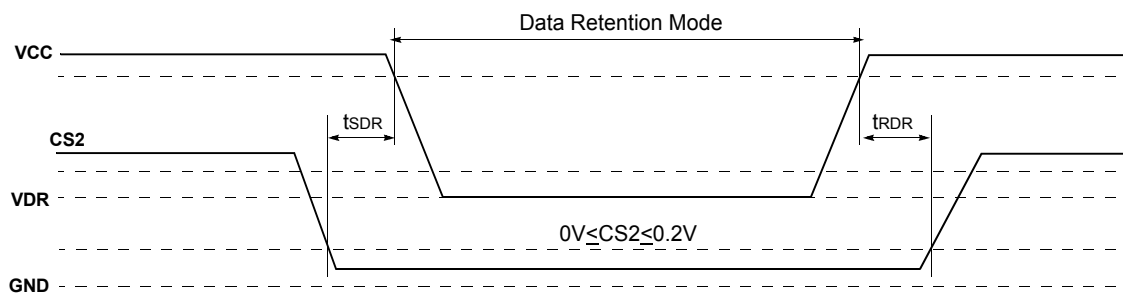
Data Retention Characteristics (TA= -40 to 85°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit	
VCC for Data Retention	VDR	Refer to Data Retention Waveform	1.5	-	-	V	
Data Retention Current	IDR	VCC=1.5V, VIN≥VCC-0.2V or VIN≤0.2V 1) CS2≤0.2V, or 2) CS2≥VCC-0.2V, CS1≥VCC-0.2V, or 3) CS2≥VCC-0.2V, CS1≤0.2V, UB=LB≥VCC-0.2V	2CS	-	2	10	μA
		VCC=1.5V, VIN≥VCC-0.2V or VIN≤0.2V 1) CS≥VCC-0.2V, or 2) CS≤0.2V, UB=LB≥VCC-0.2V	1CS				
Data Retention Set-Up Time	tSDR	Refer to Data Retention Waveform	0	-	-	ns	
Recovery Time	tRDR		tRC	-	-	ns	

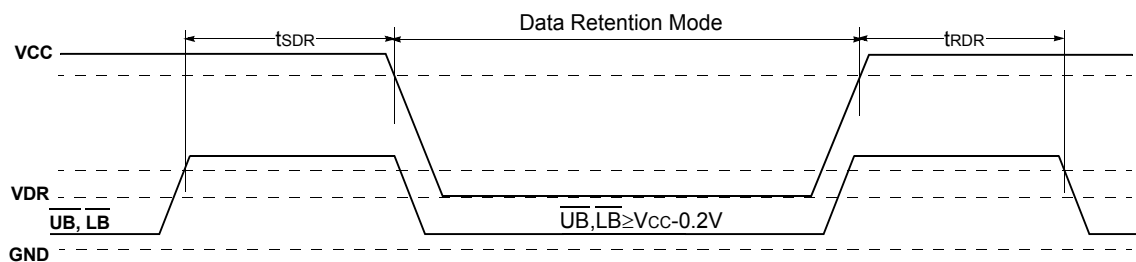
Data Retention Wave Form (1) - CS1 Controlled



Data Retention Wave Form (2) - CS2 controlled



Data Retention Wave Form (3) - UB, LB Controlled



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AC Test Conditions

Parameter	Value
Input Pulse Level	0 to 3.0V (Vcc=3.3V or 5.0V)
	0 to 2.5V (Vcc=2.5V)
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V (Vcc=3.3V or 5.0V)
	1/2Vcc (Vcc=2.5V)
Output Load	CL=30pF + 1TTL, I _{OH} /I _{OL} =-1mA/2.1mA

Read Cycle (TA= -40 to 85°C)

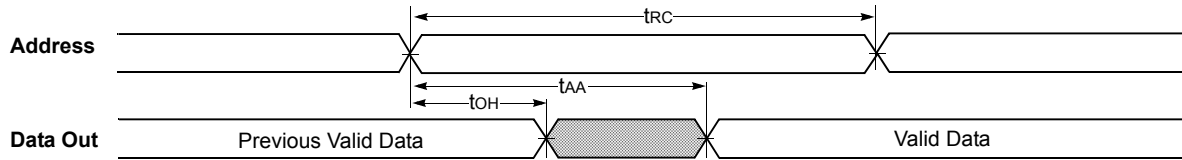
Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	45	-	55	-	70	-	ns
Address Access Time	t _{AA}	-	45	-	55	-	70	ns
Output Hold from Address Change	t _{OH}	10	-	10	-	10	-	ns
$\overline{\text{CS}}$ Low to Valid Output	t _{CO}	-	45	-	55	-	70	ns
$\overline{\text{OE}}$ Low to Valid Output	t _{OE}	-	22	-	25	-	35	ns
$\overline{\text{CS}}$ Low to Low-Z Output	t _{LZ}	10	-	10	-	10	-	ns
$\overline{\text{OE}}$ Low to Low-Z Output	t _{OLZ}	5	-	5	-	5	-	ns
$\overline{\text{CS}}$ High to High-Z Output	t _{HZ}	-	18	0	20	0	25	ns
$\overline{\text{OE}}$ High to High-Z Output	t _{OHZ}	-	18	0	20	0	25	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Access Time	t _{BA}	-	45	-	55	-	70	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Low to Low-Z Output	t _{BLZ}	5	-	5	-	5	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ High to High-Z Output	t _{BHZ}	-	18	0	20	0	25	ns

Write Cycle (TA= -40 to 85°C)

Parameter	Symbol	45ns		55ns		70ns		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	45	-	55	-	70	-	ns
$\overline{\text{CS}}$ Low to End of Write	t _{CW}	35	-	45	-	60	-	ns
Address Set-up to Start of Write	t _{AS}	0	-	0	-	0	-	ns
Address Set-up to End of Write	t _{AW}	35	-	45	-	60	-	ns
Address Hold from End of Write	t _{WR}	0	-	0	-	0	-	ns
$\overline{\text{WE}}$ Pulse Width	t _{WP}	35	-	40	-	55	-	ns
$\overline{\text{UB}}$, $\overline{\text{LB}}$ Low to End of Write	t _{BW}	35	-	45	-	60	-	ns
Data Set-up to End of Write	t _{DW}	25	-	25	-	30	-	ns
Data Hold from End of Write	t _{DH}	0	-	0	-	0	-	ns
$\overline{\text{WE}}$ Low to Output High-Z	t _{WHZ}	-	18	-	20	-	25	ns
$\overline{\text{WE}}$ High to Output Low-Z	t _{OW}	5	-	5	-	5	-	ns

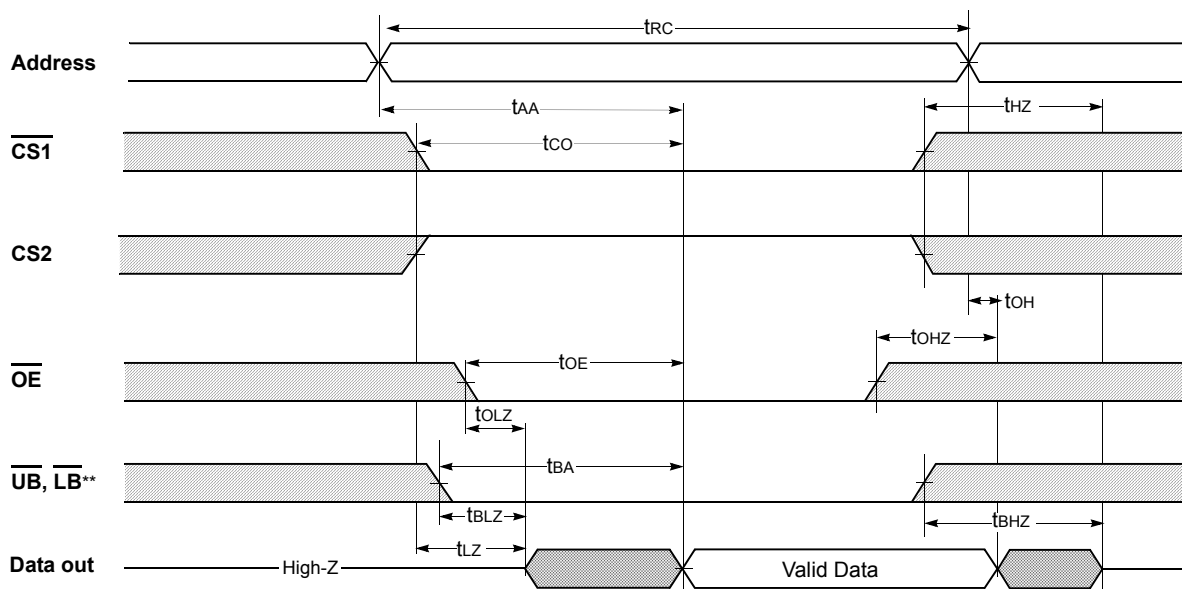
Timing Diagrams

Timing Waveform Of Read Cycle(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, $\overline{UB}=\overline{LB}=V_{IL}$ *)



* Those parameters are applied for x16 mode only.

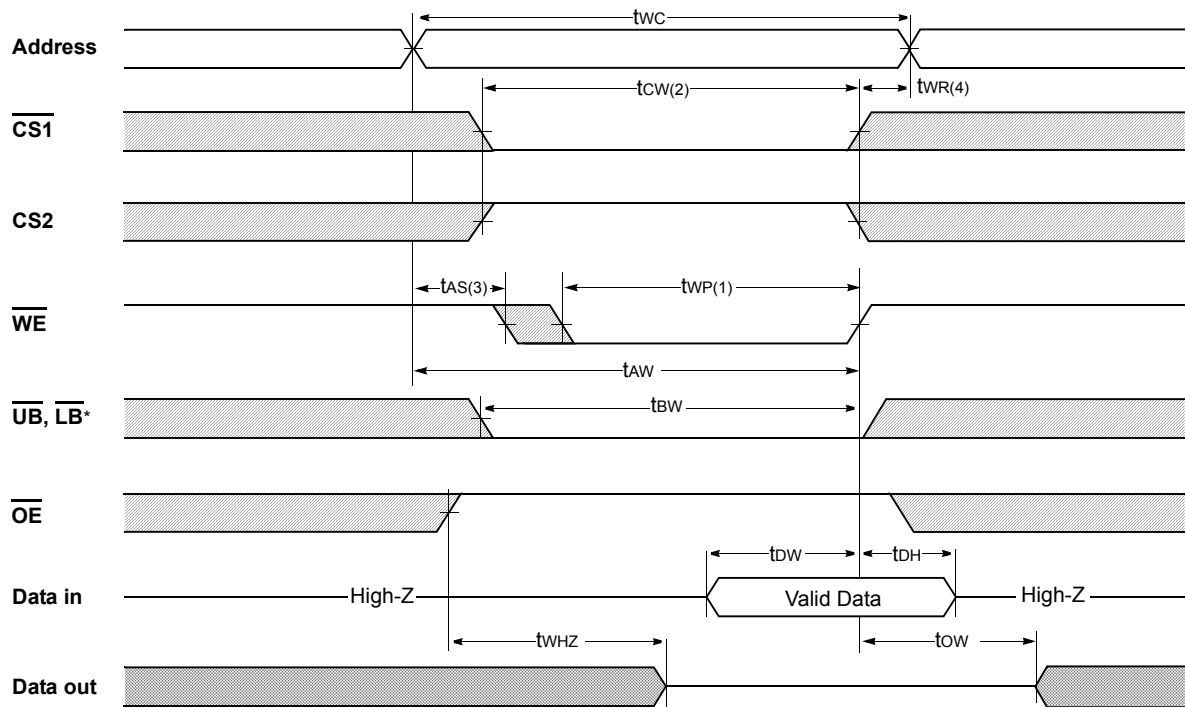
Timing Waveform Of Read Cycle(2) ($\overline{WE}=V_{IH}$, \overline{OE} Controlled)



NOTES(Read Cycle)

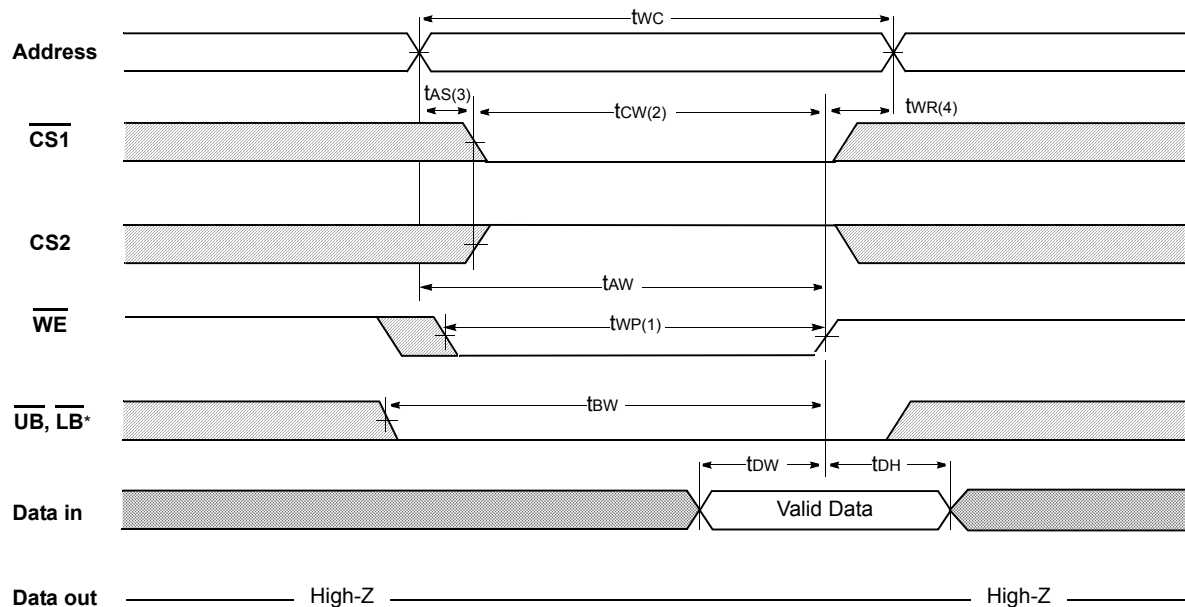
1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.

Timing Waveform Of Write Cycle(1) (\overline{WE} Controlled)



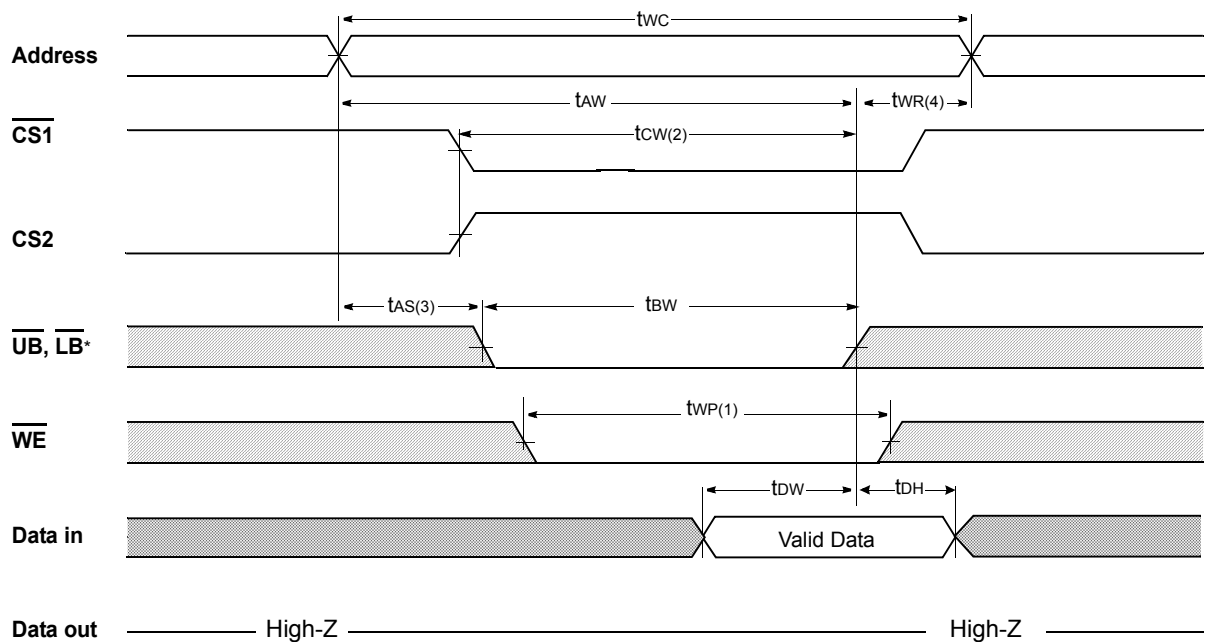
* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(2) ($\overline{CS1}$, CS2 Controlled)



* Those parameters are applied for x16 mode only.

Timing Waveform Of Write Cycle(3) (\overline{UB} , \overline{LB} Controlled)



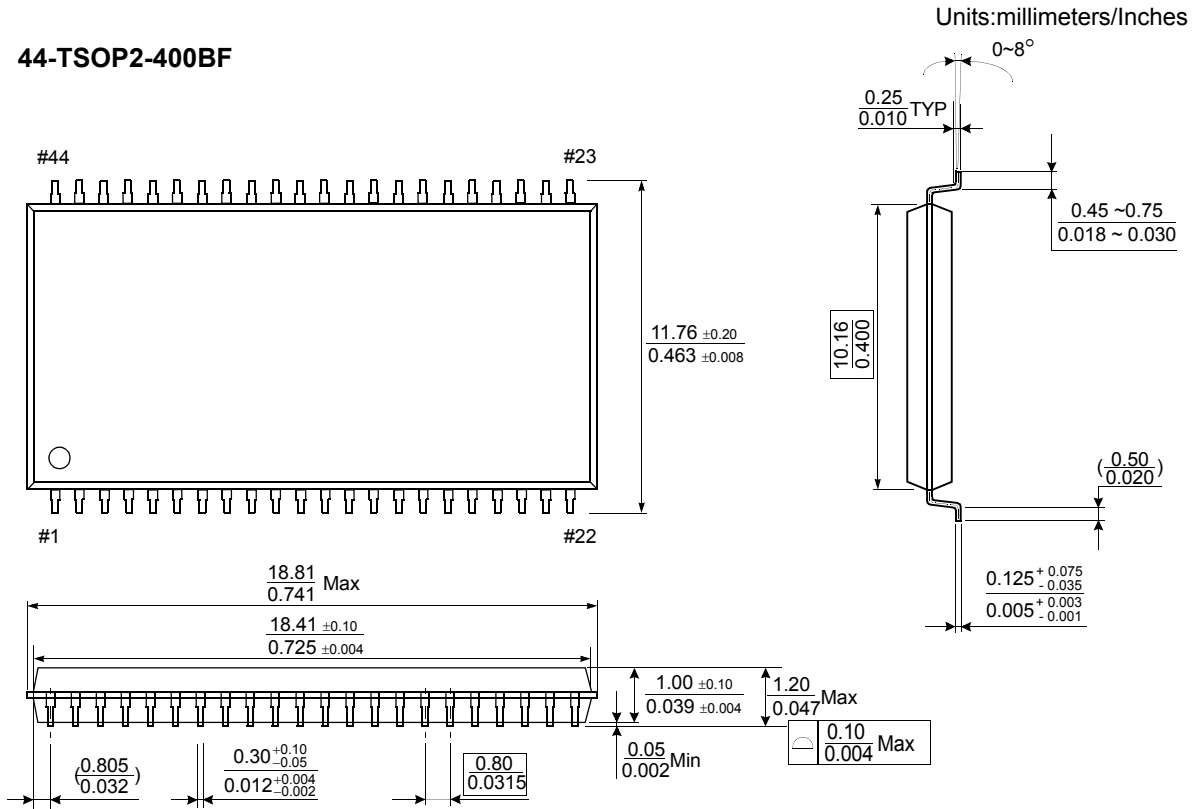
* Those parameters are applied for x16 mode only.

NOTES (Write Cycle)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS1}$ or \overline{WE} going high.

Package Dimensions

44-TSOP2-400BF



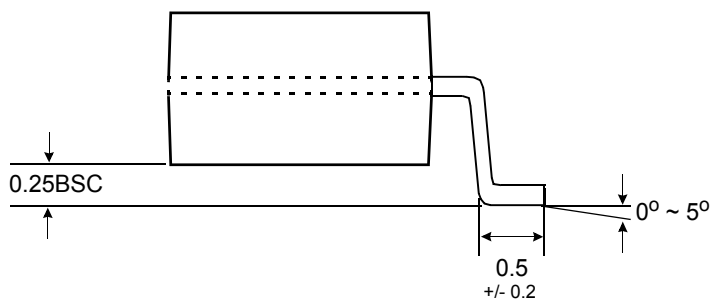
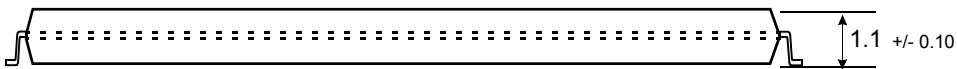
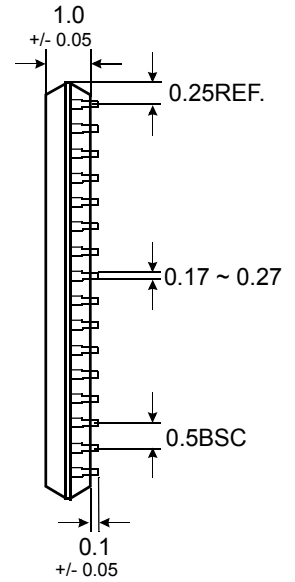
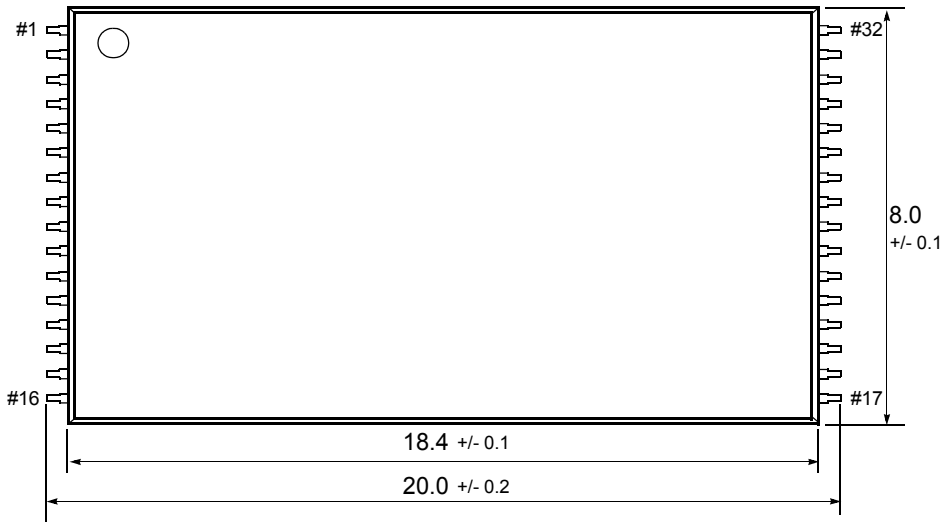
**S6L1016W, S6L1016C
S6L1008W, S6L1008C**

1M Low Power SRAM

Package Dimensions

32TSOP1

Units: millimeters



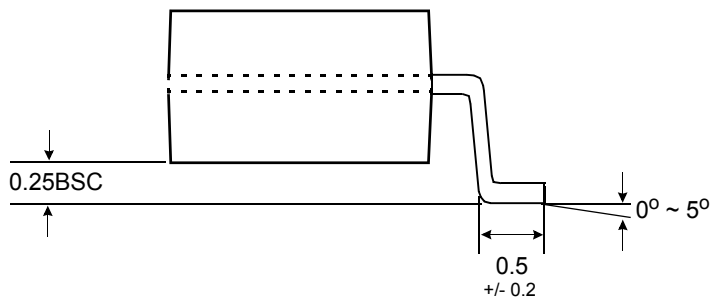
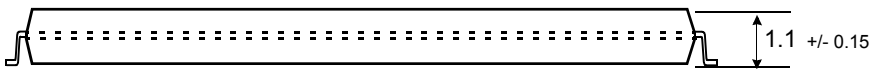
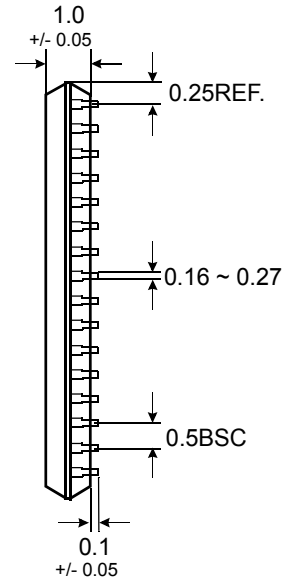
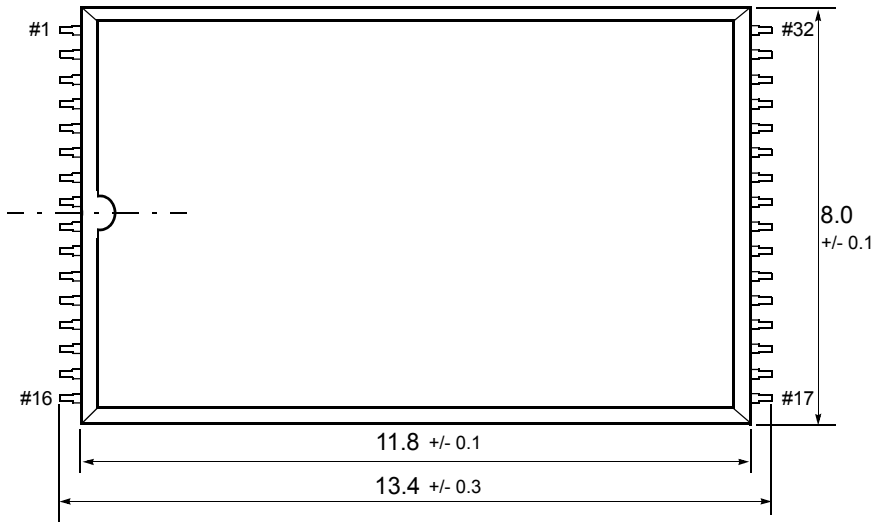
S6L1016W, S6L1016C
S6L1008W, S6L1008C

1M Low Power SRAM

Package Dimensions

32sTSOP1

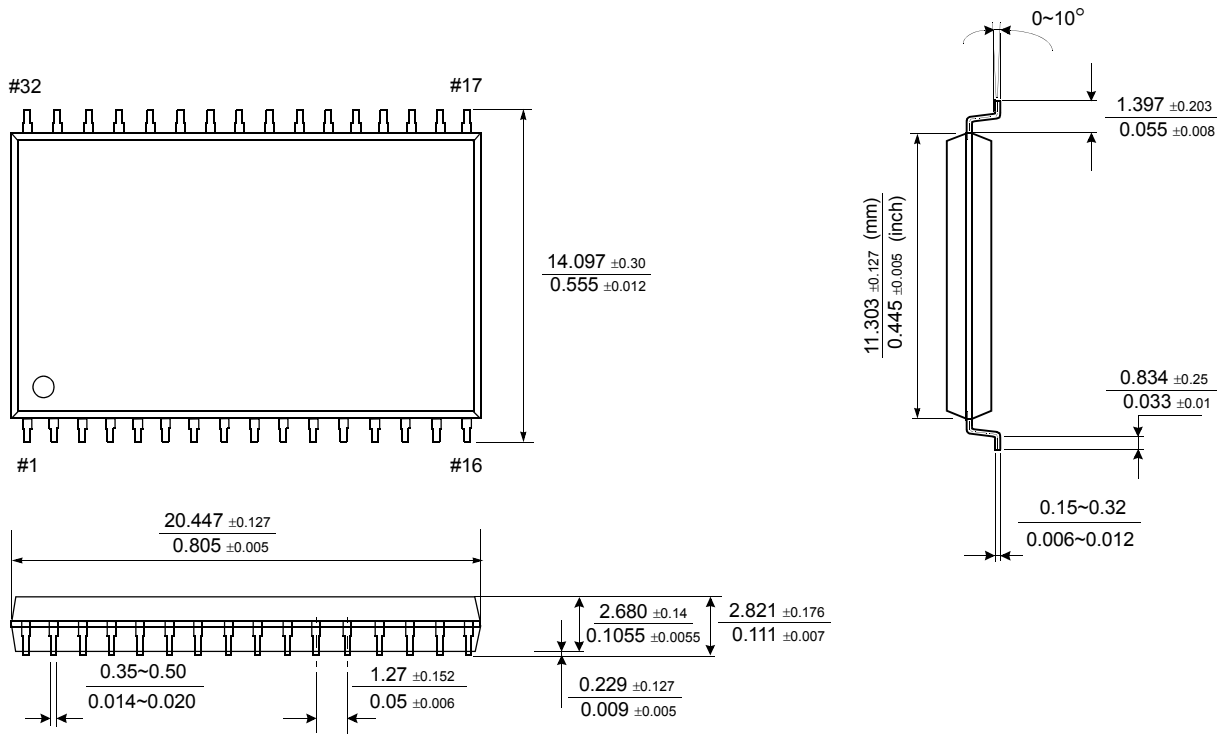
Units: millimeters



Package Dimensions

32SOP

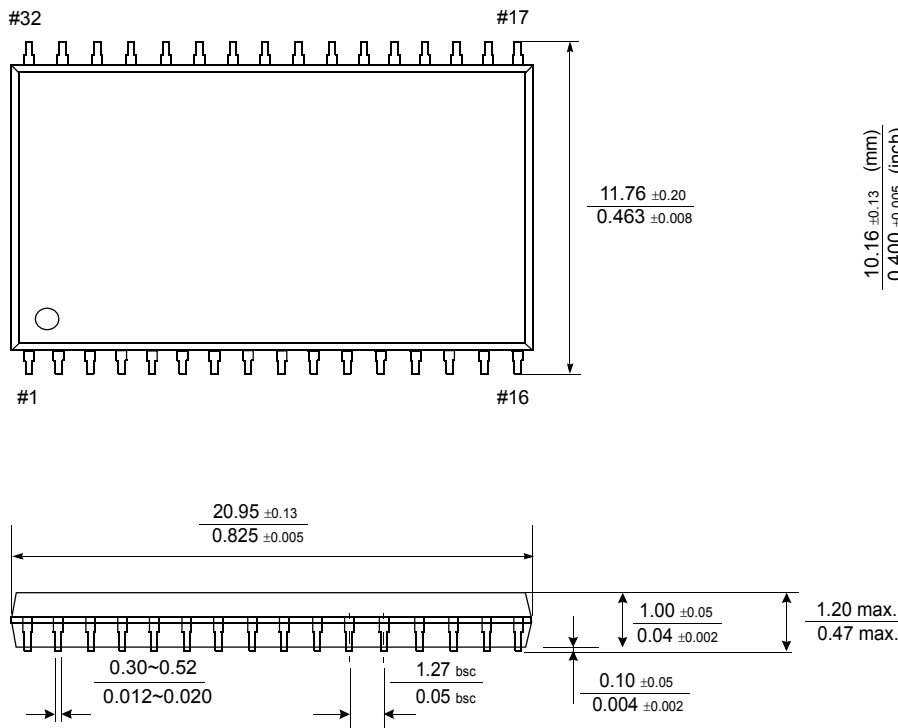
Units: millimeters/Inches



Package Dimensions

32TSOP2

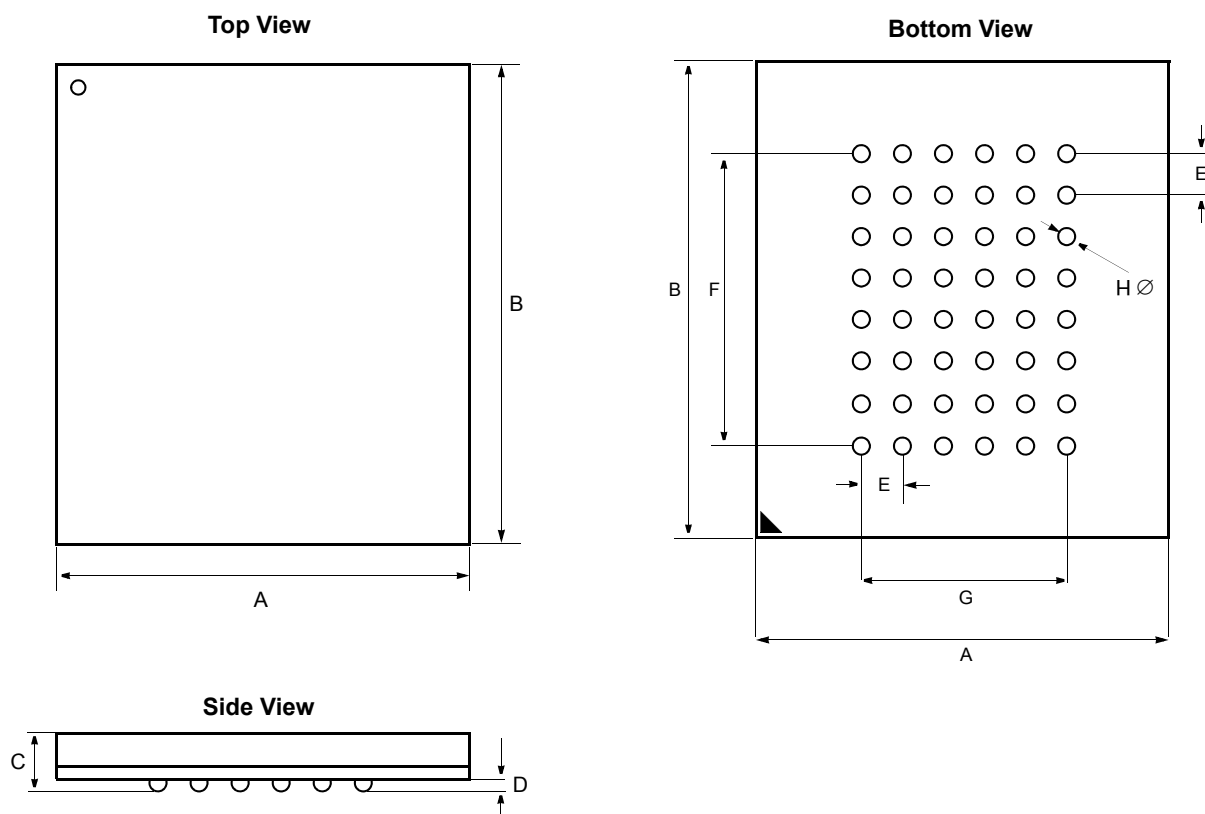
Units: millimeters/Inches



Package Dimensions

48-FBGA

6mm x 8mm Body, 0.75mm Bump Pitch, 6 x 8 Ball Grid Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	6 ± 0.1	mm		E	0.75	mm	
B	8 ± 0.1	mm		F	5.25	mm	
C	1.1 ± 0.1	mm		G	3.75	mm	
D	0.25 ± 0.05	mm		H	0.35 ± 0.05	mm	