

LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

U401 - U406

LOW NOISE LOW DRIFT
MONOLITHIC DUAL N-CHANNEL JFET

FEATURES

LOW DRIFT	$ V_{GS1-2}/T = 10\mu V/^{\circ}C$ TYP.
LOW NOISE	$e_n = 6nV/\sqrt{Hz}$ @10Hz TYP.
LOW PINCHOFF	$V_p = 2.5V$ TYP.

ABSOLUTE MAXIMUM RATINGS NOTE 1

@ 25 °C (unless otherwise noted)

Maximum Temperatures

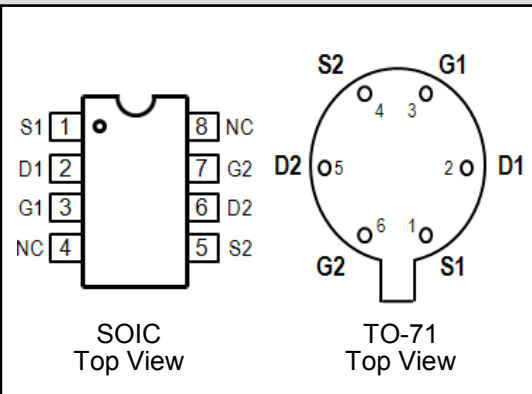
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C

Maximum Voltage and Current for Each Transistor NOTE 1

$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA

Maximum Power Dissipation per side NOTE 2

Device Dissipation $T_A = 25^{\circ}C$	300mW
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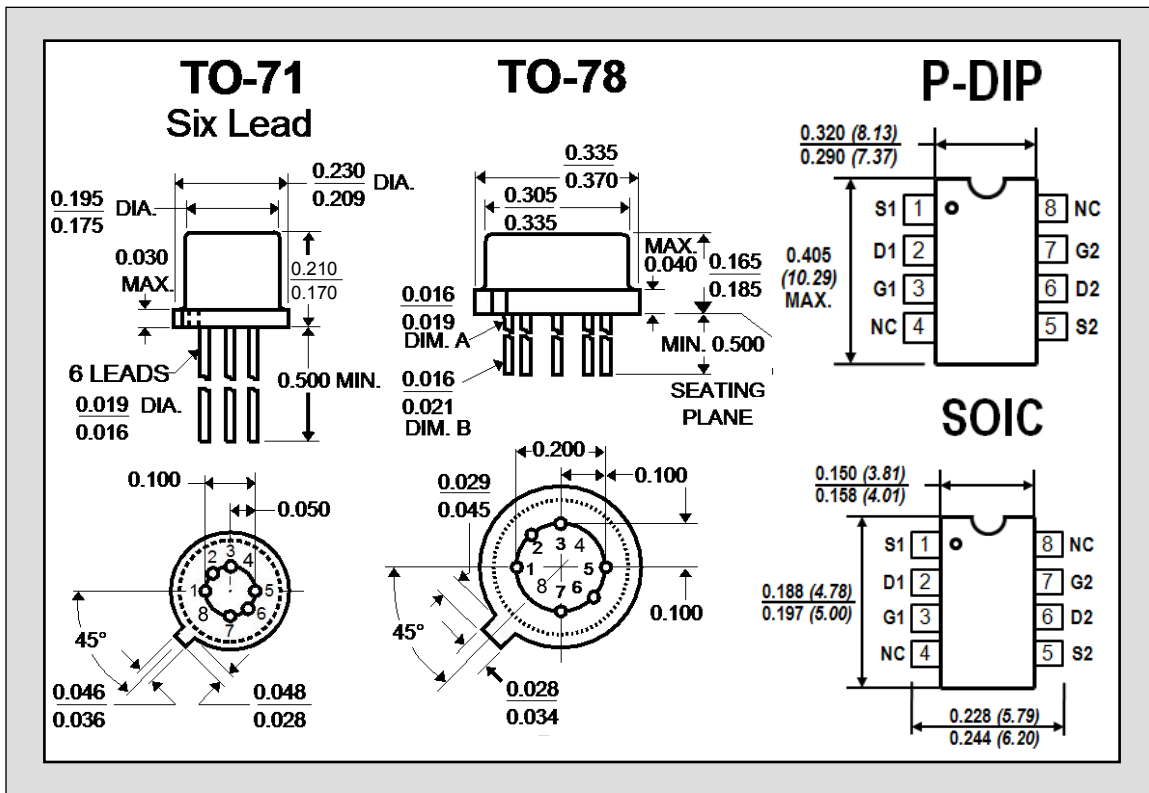
MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	U401	U402	U403	U404	U405	U406	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	Drift vs. Temperature	10	10	25	25	40	80	$\mu V/^{\circ}C$	$V_{DG} = 10V, I_D = 200\mu A$ $T_A = -55^{\circ}C$ to $+125^{\circ}C$
$ V_{GS1-2} $ max.	Offset Voltage	5	10	10	15	20	40	mV	$V_{DG} = 10V, I_D = 200\mu A$

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$ (unless otherwise noted) NOTE 3

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS		
BV_{GSS}	Breakdown Voltage	-50	-60	--	V	$V_{DS} = 0$	$I_D = 1nA$	
BV_{G1G2}	Gate-to-Gate Breakdown	± 50	--	--	V	$I_G = \pm 1\mu A$	$I_D = 0, I_S = 0$	
TRANSCONDUCTANCE								
G_{fss}	Full Conduction	2000	--	7000	μS	$V_{DG} = 10V$	$V_{GS} = 0, f = 1kHz$	
G_{fs}	Typical Operation	1000	--	2000	μS	$V_{DG} = 15V$	$I_D = 200\mu A, f = 1kHz$	
$ G_{fs1}/G_{fs2} $	Mismatch	0.97	--	1.0				
I_{DSS}	Saturation Drain Current	0.5	--	10	mA			
I_{DSS1}/I_{DSS2}	Saturation Current Ratio	0.9	0.98	1.0		$V_{DG} = 10V$	$V_{GS} = 0$	
GATE VOLTAGE								
$V_{GS(off)}$ or V_p	Pinchoff Voltage	-0.5	--	-2.5	V	$V_{DS} = 15V$	$I_D = 1nA$	
V_{GS}	Operating Range	--	--	-2.3	V	$V_{DS} = 15V$	$I_D = 200\mu A$	
GATE CURRENT								
I_G	Operating	--	-4	-15	pA	$V_{DG} = 15V$	$I_D = 200\mu A$	
I_G	High Temperature	--	--	-10	nA	$T_A = +125^{\circ}C$		
I_{GSS}	Gate Reverse Current	--	--	-100	pA	$V_{GS} = -30V, V_{DS} = 0V$		
I_{G1G2}	Gate to Gate Isolation Current	--	--	± 1.0	μA	$V_{G1} - V_{G2} = \pm 50V, I_D = I_S = 0$		

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
G _{oss}	Full Conduction	--	--	20	μS	V _{DS} = 10V, V _{GS} = 0, f = 1kHz
G _{os}	Operating	--	0.2	2	μS	V _{DS} = 15V, I _D = 500μA, f = 1kHz
	COMMON MODE REJECTION					
CMRR	$-20 \log \left \frac{\Delta V_{GS1-2}}{V_{DG}} \right $	95	--	--	dB	V _{DS} = 10 to 20V I _D =30μA
	NOISE					
NF	Figure	--	--	0.5	dB	V _{DS} = 15V V _{GS} = 0 R _G =10M f= 100Hz NBW= 6Hz
e _n	Voltage	--	20	--	nV/Hz	V _{DS} = 15V I _D = 200μA f= 10Hz NBW= 1Hz
	CAPACITANCE					
C _{ISS}	Input	--	--	8	pF	V _{DS} = 15V I _D = 200μA f= 1MHz
C _{RSS}	Reverse Transfer	--	--	1.5	pF	



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 2.4mW/°C when TA is greater than 25°C
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.