

LINEAR SYSTEMS

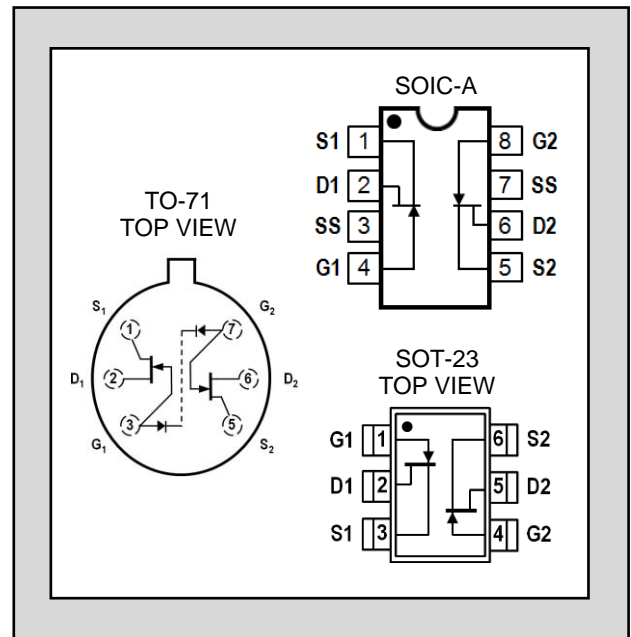
Over Three Decades of Quality Through Innovation

LSK589

LOW NOISE, LOW CAPACITANCE
MONOLITHIC DUAL
N-CHANNEL JFET

FEATURES	
ULTRA LOW NOISE	$e_n = 4.0 \text{ nV}/\sqrt{\text{Hz}}$
LOW INPUT CAPACITANCE	$C_{iss} = 5\text{pF}$
HIGH TRANSCONDUCTANCE	$G_{fs} \geq 4000\mu\text{S}$

ABSOLUTE MAXIMUM RATINGS ¹ @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side ⁴	250mW
Power Dissipation, total ⁵	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)} = 50\text{mA}$
Maximum Voltages	
Gate to Source	$V_{GS0} = 25\text{V}$
Gate to Drain	$V_{GDO} = 25\text{V}$



MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

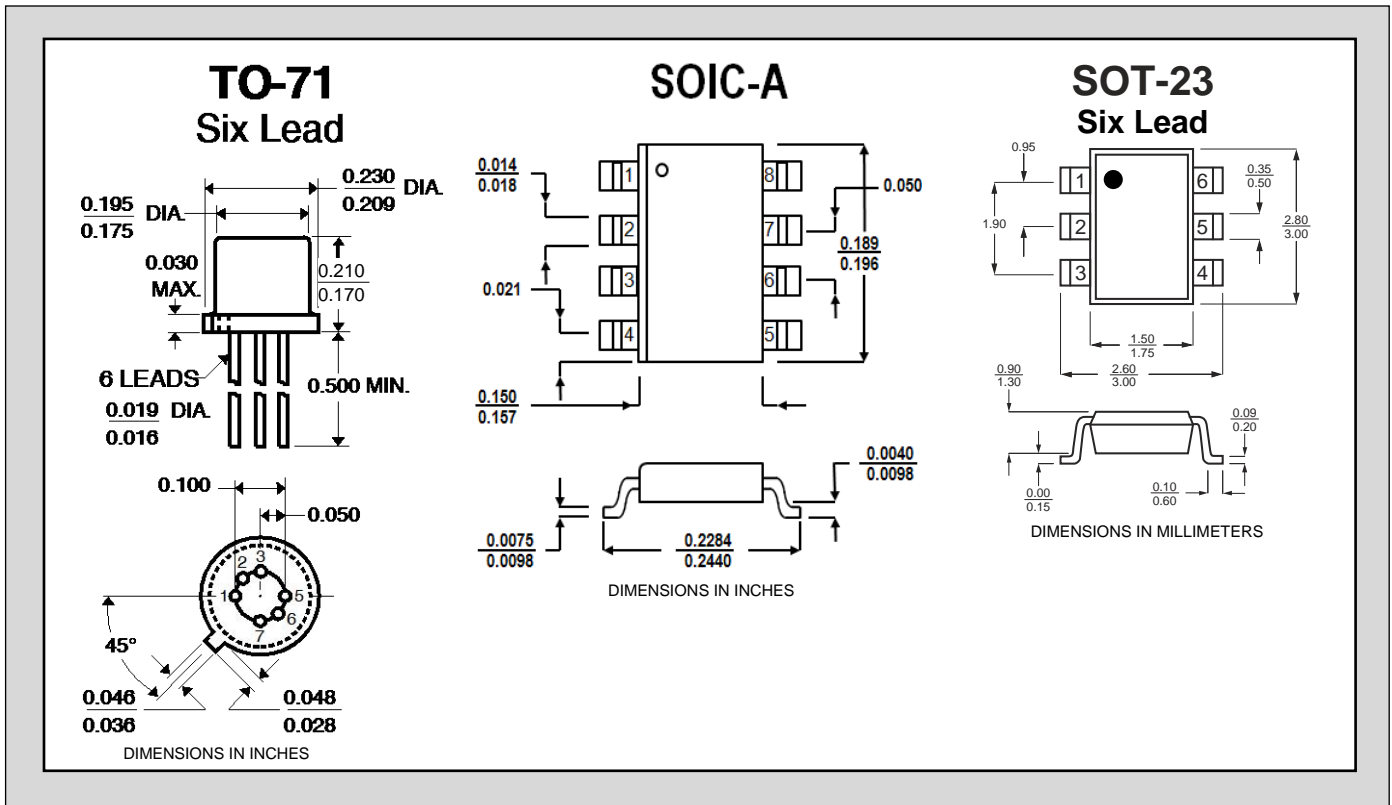
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{GS1} - V_{GS2} $	Differential Gate to Source Cutoff Voltage			20	mV	$V_{DS} = 10\text{V}, I_D = 5\text{mA}$
$\frac{I_{DSS1}}{I_{DSS2}}$	Gate to Source Saturation Current Ratio	0.9		1.0		$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$ (Note 2)
CMRR	COMMON MODE REJECTION RATIO $-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	85			dB	$V_{DG} = 5\text{V to } 10\text{V}, I_D = 5\text{mA}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
e_n	Noise Voltage		7		$\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 10\text{V}, I_D = 5\text{mA}, f = 100\text{Hz}$
e_n	Noise Voltage		4		$\text{nV}/\sqrt{\text{Hz}}$	$V_{DS} = 10\text{V}, I_D = 5\text{mA}, f = 10\text{kHz}$
C_{ISS}	Common Source Input Capacitance			5	pF	$V_{DS} = 10\text{V}, I_D = 5\text{mA}, f = 1\text{MHz}$
C_{RSS}	Common Source Reverse Transfer Capacitance			1.2	pF	

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GS}	Gate to Source Breakdown Voltage	-25			V	$V_{DS} = 0, I_D = 1\mu A$
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	-1.5		-5	V	$V_{DS} = 10V, I_D = 1nA$
V_{GS}	Gate to Source Operating Voltage	-0.3		-4.0	V	$V_{DS} = 10V, I_D = 5mA$
I_{DSS}	Drain to Source Saturation Current	7.0		40	mA	$V_{DS} = 10V, V_{GS} = 0V$ (Note 2)
I_G	Gate Operating Current		-1	-50	μA	$V_{DG} = 10V, I_D = 5mA$
I_{GSS}	Gate to Source Leakage Current			-50	μA	$V_{GS} = -15V, V_{DS} = 0$
G_{OS}	Output Conductance $F = 1kHz$			100	μS	$V_{DS} = 10V, I_D = 5mA$
NF	Noise Figure			1.0	dB	$V_{DS} = 10V, I_D = 5mA, R_G = 100K\Omega, f = 100Hz$
G_{fs}	Forward Transconductance	$f = 1kHz$	4000	10000	μS	$V_{DS} = 10V, I_D = 5mA$
		$f = 100MHz$		7000		
G_{os}	Output Transconductance	$f = 1kHz$		100		
		$f = 100MHz$		120		

PACKAGE DIMENSIONS



NOTES:

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse Test: $PW \leq 300 \mu s$, Duty Cycle $\leq 3\%$
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.0 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

Linear Integrated Systems (LIS), established in 1987, is a third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company Founder John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.