LINEAR SYSTEMS

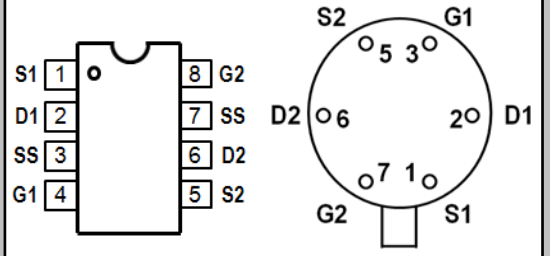
Twenty-Five Years Of Quality Through Innovation

LS840 LS841 LS842

LOW NOISE LOW DRIFT LOW CAPACITANCE MONOLITHIC DUAL N-CHANNEL JFET

FEATURES	
LOW NOISE	e_n=8nV/Hz TYP.
LOW LEAKAGE	I_G=10pA TYP.
LOW DRIFT	I V_{GS1-2}/TI=5µV/ºC max.
LOW OFFSET VOLTAGE	IV_{GS1-2}I=2mV TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55°C to +150°C
Operating Junction Temperature		-55°C to +150°C
Maximum Voltage and Current for Each Transistor[1]		
-V_{GSS}	Gate Voltage to Drain or Source	60V
$I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation		
Device Dissipation[2] @ Free Air - Total		400mW T_A=+25°C



SOIC Top View

TO-71/78 Top View

ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS840	LS841	LS842	UNITS	CONDITIONS
I V_{GS1-2} / TI max.	Drift vs. Temperature	5	10	40	µV/ºC	V_{DG} = 20V I_D = 200µA T_A = -55ºC to +125ºC
IV_{GS1-2}I max.	Offset Voltage	5	10	25	mA	V_{DG} = 20V I_D = 200µA

SYMBOL	CHARACTERISTIC[3]	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-60	--	--	V	V_{DS}= 0 I_D= -1nA
BV_{GGO}	Gate-to-Gate Breakdown	±60	--	--	V	I_{GGO}= ±1µA I_D= 0 I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	1000		4000	µS	V_{DG}= 20V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Conduction	500		1000	µS	V_{DG}= 20V I_D= 200µA
$\frac{G_{fs1}}{G_{fs2}}$ [4]	Mismatch Transconductance Ratio	0.97		1.0		
	DRAIN CURRENT					
I_{DSS}	Full Conduction	0.5	2	5	mA	V_{DG}= 20V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$ [4]	Drain Current Ratio	0.95		1.0		
	GATE-SOURCE					
V_{GS}(off)	Pinchoff Voltage	-1	-2	-4.5	V	V_{DS}= 20V I_D= 1nA
V_{GS}	Operating Range	-0.5	--	-4	V	V_{DS}= 20V I_D= 200µA
	GATE CURRENT					
-I_G	Operating	--	10	50	pA	V_{DG}= 20V I_D =200µA
-I_G	High Temperature	--	--	50	nA	V_{DG}= 20V I_D =200µA T_A=+125ºC
-I_G	Reduced VDG	--	5	--	pA	V_{DG}= 10V I_D =200µA
-I_{GSS}	At Full Conduction	--	--	100	pA	V_{DG}= 20V V_{DS} =0

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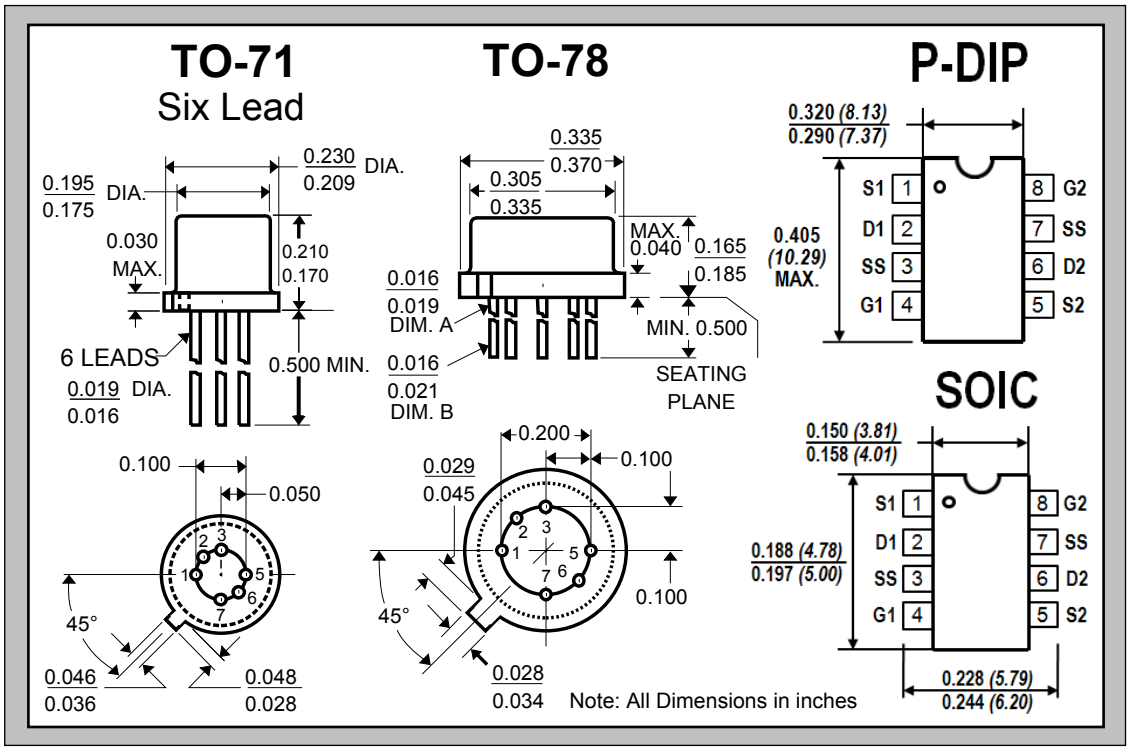
Doc 201143 8/16/2012 Rev#A7 ECN# LS840 LS841 LS842

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
G_{OSS}	Full Conduction	--	--	10	µS	V_{DG}= 20V V_{GS}= 0
G_{OS}	Operating	--	0.1	1	µS	V_{DG}= 20V I_D= 200µA
$\lvert G_{OS\ 1\text{-}2} \rvert$	Differential	--	0.01	0.1	µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert V_{GS1\text{-}2} / V_{DS} \rvert$	--	100	--	dB	V_{DS}= 10 to 20V I_D=200µA
CMRR		--	75	--	dB	V_{DS}= 5 to 10V I_D=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 20V V_{GS}= 0 R_G=10M f= 100Hz NBW= 6Hz
e_n	Voltage	--	--	10	nV/Hz	V_{DS}= 20V I_D= 200µA f= 1KHz NBW= 1Hz
e_n	Voltage	--	--	15	nV/Hz	V_{DS}= 20V I_D= 200µA f= 10Hz NBW= 1Hz
	CAPACITANCE					
C_{ISS}	Input	--	4	10	pF	V_{DS}= 20V I_D=200µA
C_{RSS}	Reverse Transfer	--	1.2	5	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	V_{DG}= 20V I_D= 200µA



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/ºC above 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.
4. Assumes smaller number in the numerator.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.

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