

LINEAR SYSTEMS

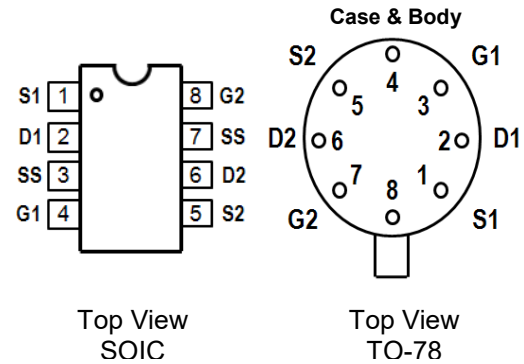
Twenty-Five Years Of Quality Through Innovation

FEATURES

LOW DRIFT	$ \Delta V_{GS1-2}/\Delta T = 5\mu V/^{\circ}C$ max.
ULTRA LOW LEAKAGE	$I_G = 150fA$ TYP.
LOW PINCHOFF	$V_P = 2V$ TYP.
ABSOLUTE MAXIMUM RATINGS¹	
@ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C
Maximum Voltage and Current for Each Transistor¹	
-V _{GSS}	Gate Voltage to Drain or Source 40V
-I _{G(f)}	Gate Forward Current 10mA
-I _G	Gate Reverse Current 10µA
Maximum Power Dissipation	
Device Dissipation @ TA=25°C - Total	500mW ²

LS5905 LS5906 LS5907 LS5908 LS5909

LOW LEAKAGE LOW DRIFT
MONOLITHIC DUAL N-CHANNEL JFET

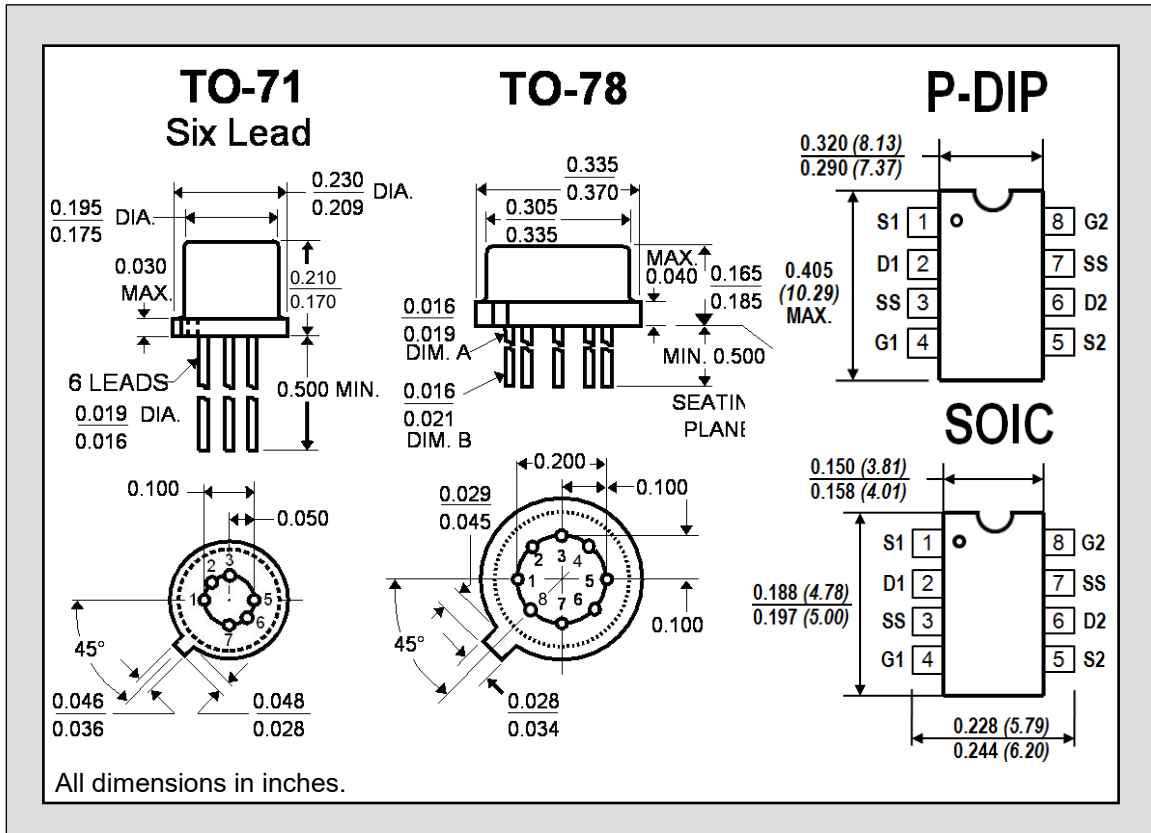


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS5906	LS5907	LS5908	LS5909	LS5905	UNITS	CONDITIONS
$ \Delta V_{GS1-2}/\Delta T $ max.	Drift vs. Temperature	5	10	20	40	40	µV/°C	V _{DS} = 10V, I _D = 30µA T _A = -55°C to +125°C
$ V_{GS1-2} $ max.	Offset Voltage	5	5	10	15	15	mV	V _{DS} = 10V I _D = 30µA
-I _G Max	Operating	1	1	1	1	3	pA	
-I _G Max	High Temperature	1	1	1	1	3	nA	T _A = +125 °C
-I _{GSS} Max	Gate Reverse Current	2	2	2	2	5	pA	V _{DS} = 0V V _{GS} = -20V
-I _{GSS} Max	Gate Reverse Current	5	5	5	5	10	nA	T _A = +125 °C

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	-40	-60	--	V	V _{DS} = 0 I _D = -1µA
BV _{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I _{GG} = ±1µA I _D = 0 I _S = 0
TRANSCONDUCTANCE						
G _{fss}	Full Conduction	70	300	500	µS	V _{DS} = 10V V _{GS} = 0 f = 1kHz
G _{fs}	Typical Operation	50	100	200	µS	V _{DS} = 10V I _D = 30µA f = 1kHz
$ G_{fs1}/G_{fs2}^3 $	Transconductance Ratio	--	1	5	%	
DRAIN CURRENT						
I _{DSS}	Full Conduction	60	400	1000	µA	V _{DS} = 10V V _{GS} = 0
$ I_{DSS1}/I_{DSS2}^3 $	Drain Current Ratio	--	2	5	%	
GATE VOLTAGE						
V _{GS(off)}	Gate-Source Cutoff Voltage	-0.6	-2	-4.5	V	V _{DS} = 10V I _D = 1nA
V _{GS}	Operating Range	--	--	-4	V	V _{DS} = 10V I _D = 30µA
GATE CURRENT						
I _{GGO}	Gate-to-Gate Leakage	--	±1	--	pA	V _{GG} = 20V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
OUTPUT CONDUCTANCE						
g_{oss}	Full Conduction	--	--	5	μS	$V_{DG}=10V$ $V_{GS}=0$
g_{os}	Operating	--	0.1	--	μS	$V_{DG}=10V$ $I_D=30\mu A$
$ g_{os1-2} $	Differential	--	0.01	0.2	μS	
COMMON MODE REJECTION						
CMRR	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	90	--	dB	$\Delta V_{DS}=10$ to $20V$ $I_D=30\mu A$
CMRR	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	90	--	dB	$\Delta V_{DS}=5$ to $10V$ $I_D=30\mu A$
NOISE						
NF	Figure	--	--	1	dB	$V_{DS}=10V$ $V_{GS}=0$ $R_G=10M\Omega$ $f=100Hz$ $NBW=6Hz$
e_n	Voltage	--	20	70	nV/\sqrt{Hz}	$V_{DS}=10V$ $I_D=30\mu A$ $f=10Hz$ $NBW=1Hz$
CAPACITANCE						
C_{ISS}	Input	--	--	3	pF	$V_{DS}=10V$ $V_{GS}=0$ $f=1MHz$
C_{RSS}	Reverse Transfer	--	--	1.5	pF	$V_{DS}=10V$ $V_{GS}=0$ $f=1MHz$
C_{DD}	Drain-to-Drain	--	--	0.1	pF	$V_{DG}=20V$ $I_D=30\mu A$ $f=1MHz$



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired
2. Derate 4mW/°C above 25°C
3. Assume smaller value in the numerator.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.