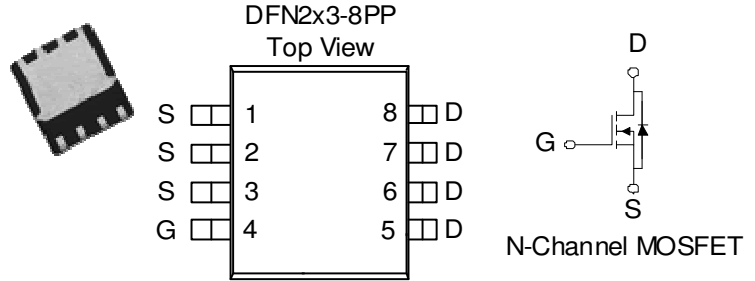


N-Channel 80-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN2x3-8PP saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
80	82 @ $V_{GS} = 10V$	± 5.4
	115 @ $V_{GS} = 4.5V$	± 4.6



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A=25^\circ C$	± 5.4
		$T_A=70^\circ C$	± 4.4
Pulsed Drain Current ^b	I_{DM}	± 25	A
Continuous Source Current (Diode Conduction) ^a	I_S	2	A
Power Dissipation ^a	P_D	$T_A=25^\circ C$	3.5
		$T_A=70^\circ C$	2
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	t <= 10 sec	35
		Steady State	81

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.6 \text{ A}$			86	m Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$			115	
Forward Transconductance ^A	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 4.6 \text{ A}$		11		S
Diode Forward Voltage	V_{SD}	$I_S = 2.0 \text{ A}, V_{GS} = 0 \text{ V}$		1.1		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V},$ $I_D = 4.6 \text{ A}$		3.6		nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 30 \Omega, I_D = 1 \text{ A},$ $V_{GEN} = 10 \text{ V}$		9		nS
Rise Time	t_r			10		
Turn-Off Delay Time	$t_{d(off)}$			21		
Fall-Time	t_f			8		

Notes

- Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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