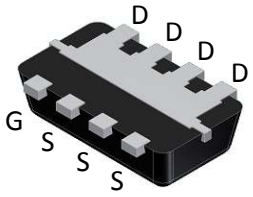
N-Channel 60-V (D-S) MOSFET

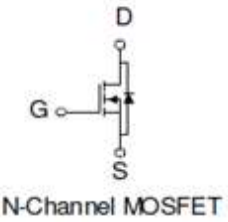
Key Features:
- Low $r_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- Small Footprint DFN3x2-8L package

Typical Applications:
- Telecom DC/DC converters
- White LED boost converters
- Industrial DC/DC conversion
- Automotive Entertainment and GPS DC/DC conversion

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (mΩ)	I_D(A)
60	82 @ V_{GS} = 10V	5
	115 @ V_{GS} = 4.5V	4.1

DFN3x2-8L EP





ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		**Symbol**	**Limit**	**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current [a]	T_A=25°C	I_D	5	A
	T_A=70°C		3.7	
Pulsed Drain Current [b]		I_{DM}	30	
Continuous Source Current (Diode Conduction) [a]		I_S	4.3	A
Power Dissipation [a]	T_A=25°C	P_D	3.5	W
	T_A=70°C		2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient [a]	t <= 10 sec	$R_{\theta JA}$	35	°C/W
	Steady State		81	

Notes

a. Surface Mounted on 1” x 1” FR4 Board.

b. Pulse width limited by maximum junction temperature

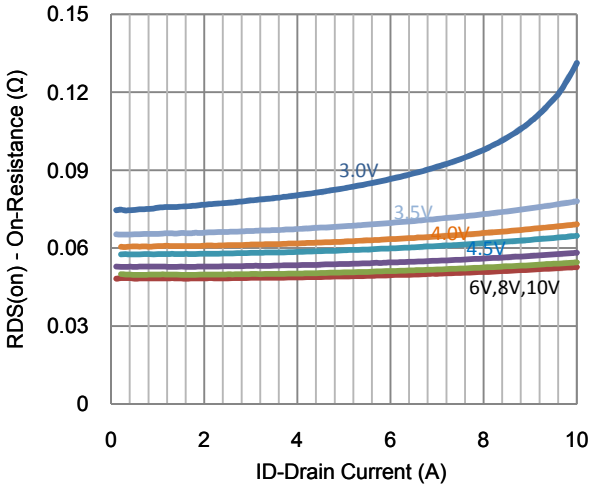
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, ID = 250 uA	1	1.5	3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	uA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	10			A
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4 A			82	mΩ
		V_{GS} = 4.5 V, I_D = 3.3 A			115	
Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 4 A		10		S
Diode Forward Voltage	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V		0.77		V
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 4 A		4.1		nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 7.5 Ω , I_D = 4 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		2.5		nS
Rise Time	t_r			4.1		
Turn-Off Delay Time	$t_{d(off)}$			12.1		
Fall-Time	t_f			4.5		

Notes

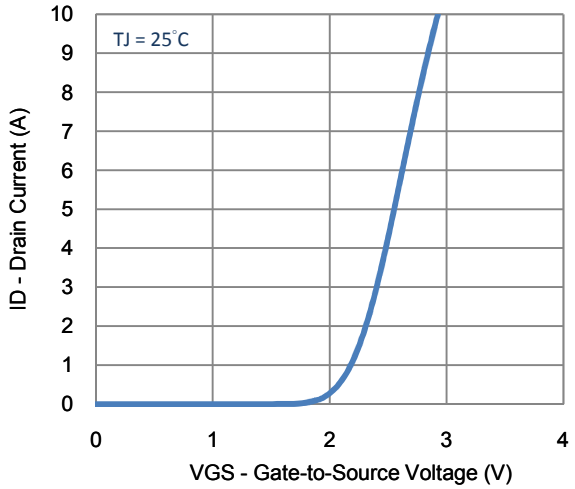
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

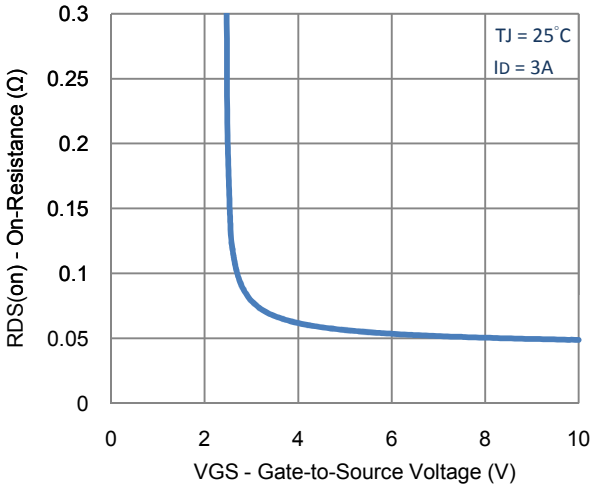
Typical Electrical Characteristics



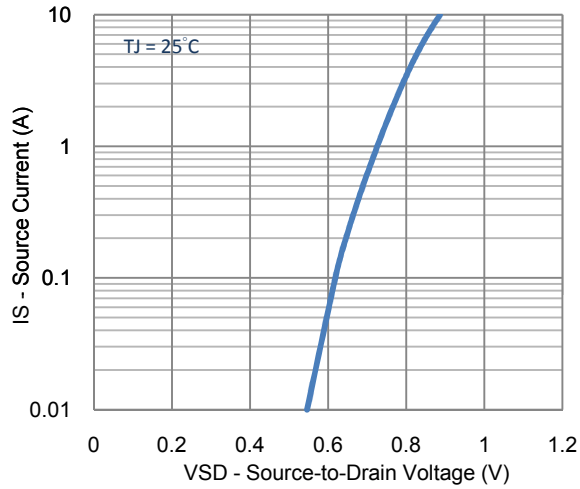
1. On-Resistance vs. Drain Current



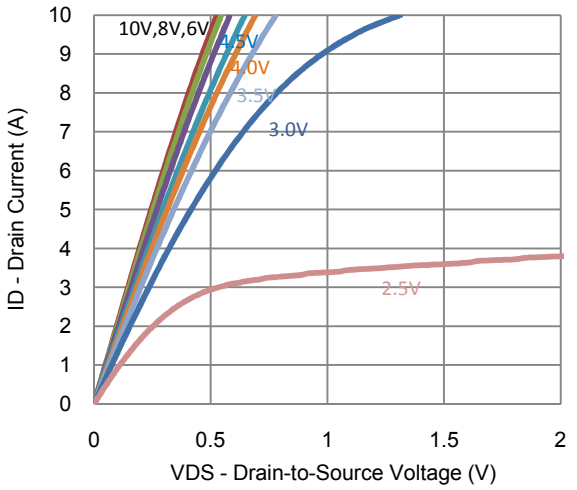
2. Transfer Characteristics



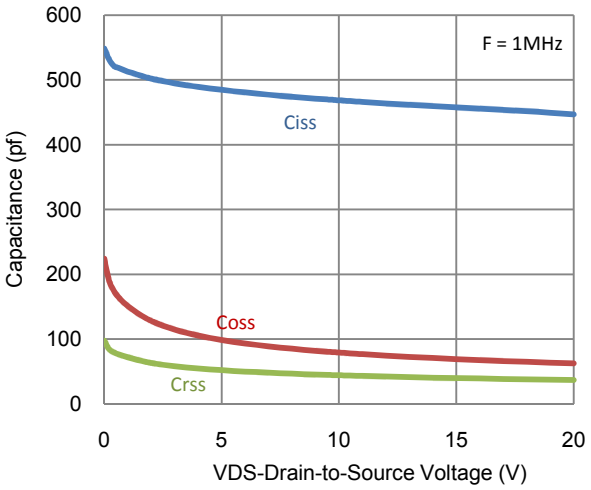
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

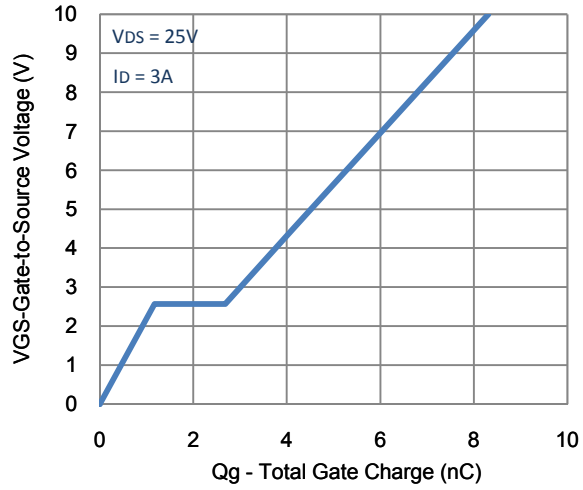


5. Output Characteristics

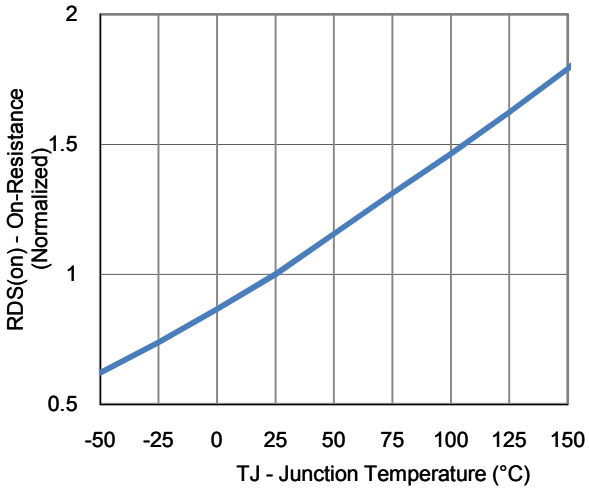


6. Capacitance

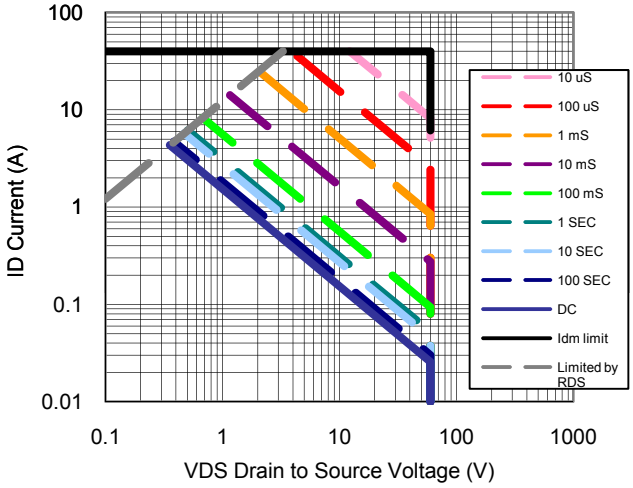
Typical Electrical Characteristics



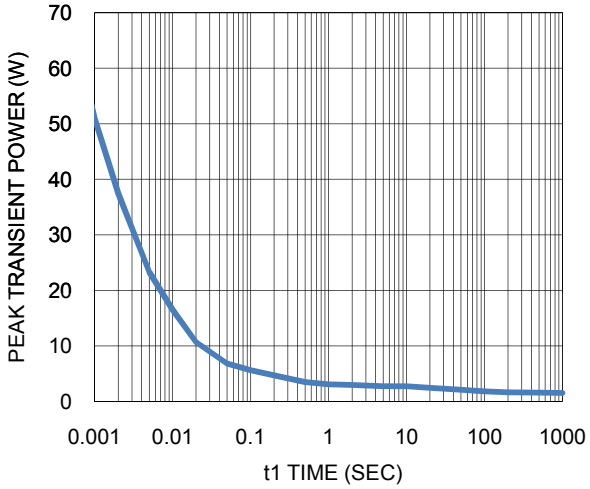
7. Gate Charge



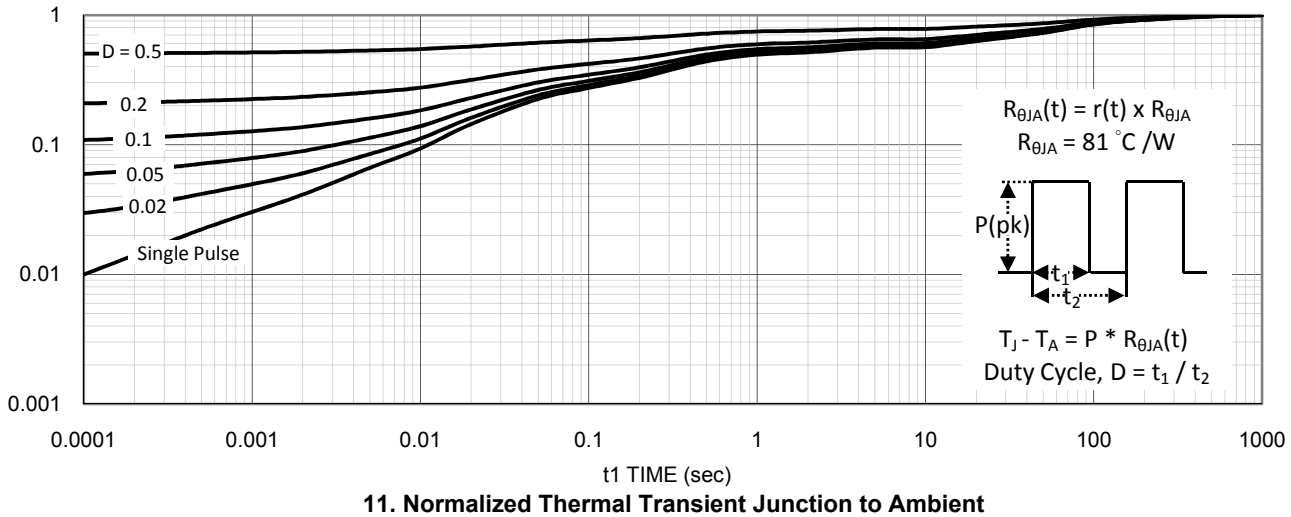
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

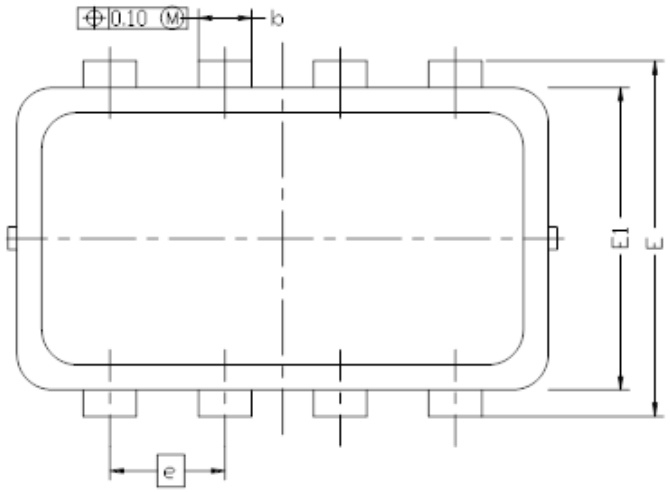


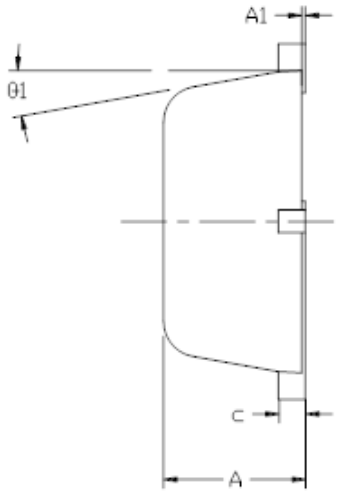
10. Single Pulse Maximum Power Dissipation

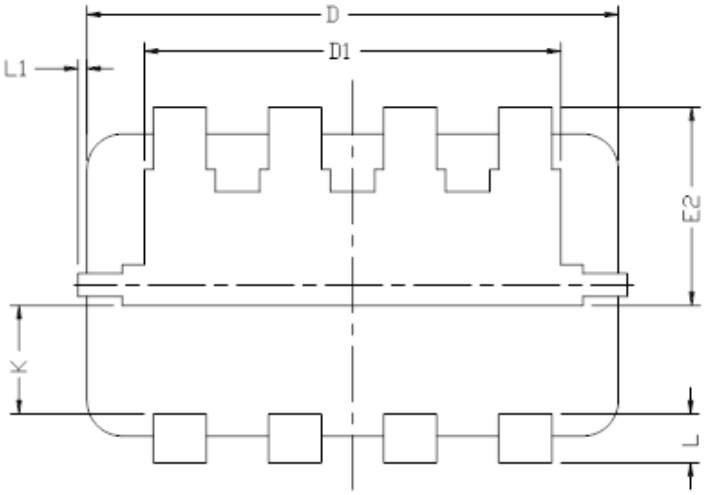


11. Normalized Thermal Transient Junction to Ambient

Package Information







DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.152	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.30	2.35	2.40	0.091	0.093	0.095
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
E2	1.065	1.115	1.165	0.042	0.044	0.046
e	0.65 BSC			0.026 BSC		
L	0.20	0.275	0.400	0.008	0.011	0.0157
K	0.56	0.61	0.66	0.022	0.024	0.026
L1	0	---	0.100	0	---	0.004
θ1	0?	10?	12?	0?	10?	12?

Note:
1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.