

P-Channel 20-V (D-S) MOSFET

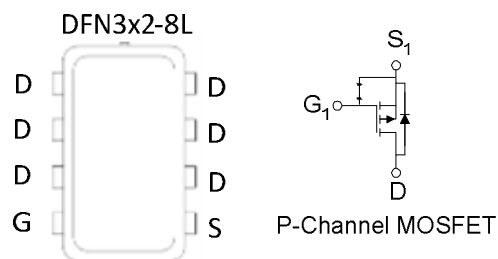
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DFN3x2-8L saves board space
- Fast switching speed
- High performance trench technology



RoHS
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FREE

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (OHM)	I _D (A)
-20	0.024 @ V _{GS} = -4.5V	-8.4
	0.031 @ V _{GS} = -2.5V	-7.4
	0.041 @ V _{GS} = -1.8V	-6.4



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V _{DS}	-20	V
Gate-Source Voltage	V _{GS}	±8	
Continuous Drain Current ^a	I _D	T _A =25°C	-8.4
		T _A =70°C	-6.9
Pulsed Drain Current ^b	I _{DM}	-60	A
Continuous Source Current (Diode Conduction) ^a	I _S	±2.5	A
Power Dissipation ^a	P _D	T _A =25°C	2.5
		T _A =70°C	1.6
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R _{THJA}	t ≤ 5 sec	50
		Steady-State	90

Notes

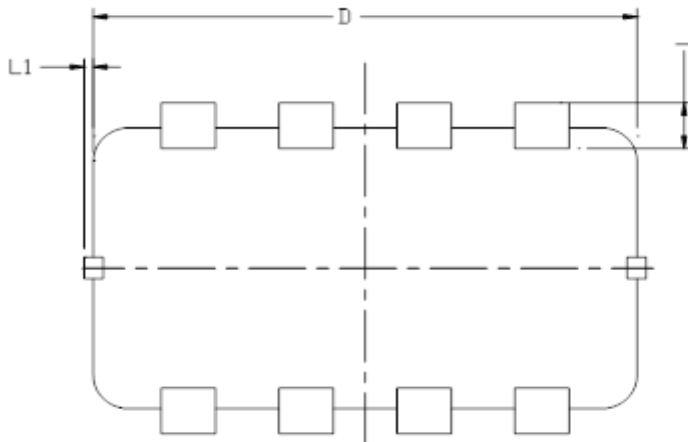
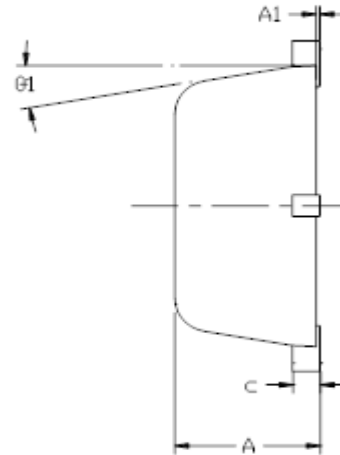
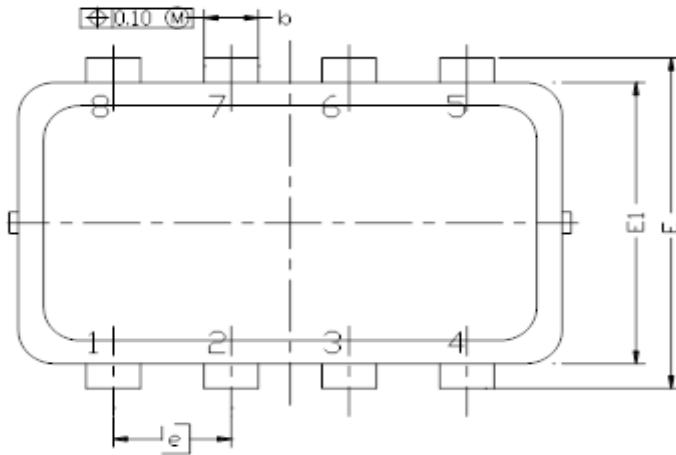
- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-0.3			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +/-8 V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-10	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-60			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -8.4 A			0.024	Ω
		V _{GS} = -2.5 V, I _D = -7.4 A			0.031	
		V _{GS} = -1.8 V, I _D = -6.4 A			0.041	
Forward Transconductance ^A	g _{fs}	V _{DS} = -5 V, I _D = -8.4 A		45		S
Diode Forward Voltage	V _{SD}	I _S = -1 A, V _{GS} = 0 V		-0.5		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -5 V, V _{GS} = -4.5 V, I _D = -8.4 A		19		nC
Gate-Source Charge	Q _{gs}			5		
Gate-Drain Charge	Q _{gd}			5		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -5 V, R _L = 5 OHM, V _{GEN} = -4.5 V, R _G = 6 OHM		240		ns
Rise Time	t _r			580		
Turn-Off Delay Time	t _{d(off)}			7		
Fall-Time	t _f			4		

Notes

- Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

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DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.08	0.152	0.25	0.003	0.006	0.010
D	3.00 BSC			0.118 BSC		
E	2.00 BSC			0.079 BSC		
E1	1.70 BSC			0.067 BSC		
e	0.65 BSC			0.026 BSC		
L	0.20	0.275	0.400	0.008	0.011	0.0157
L1	0	---	0.100	0	---	0.004
θ1	0°	10°	12°	0°	10°	12°

Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.
4. The Package Top May Be Smaller Than The Package Bottom.