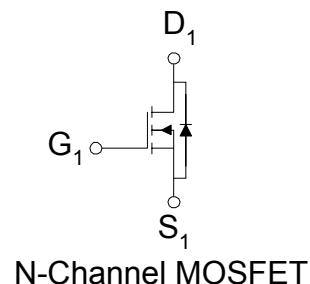
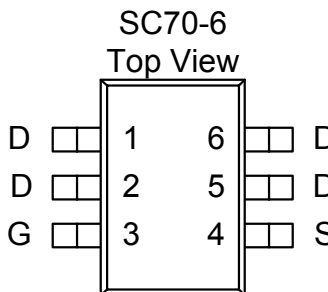


N-Channel 40V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
40	0.086 @ $V_{GS} = 10\text{ V}$	3.5
	0.128 @ $V_{GS} = 4.5\text{ V}$	2.9

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SC70-6 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	$T_A = 25^\circ\text{C}$	3.5
		$T_A = 70^\circ\text{C}$	2.9
Pulsed Drain Current ^b	I_{DM}	± 20	A
Continuous Source Current (Diode Conduction) ^a	I_S	1.6	
Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.56
		$T_A = 70^\circ\text{C}$	0.81
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	R_{THJA}	$t \leq 5\text{ sec}$	100
		Steady-State	166

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 32\ \text{V}, V_{GS} = 0\ \text{V}$			1	uA
		$V_{DS} = 32\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^A	$I_{D(on)}$	$V_{DS} = 5\ \text{V}, V_{GS} = 4.5\ \text{V}$	10			A
Drain-Source On-Resistance ^A	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 3.5\ \text{A}$			86	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 2.9\ \text{A}$			128	
Forward Transconductance ^A	g_s	$V_{DS} = 10\ \text{V}, I_D = 3.5\ \text{A}$		11.3		S
Diode Forward Voltage	V_{SD}	$I_S = 1.6\ \text{A}, V_{GS} = 0\ \text{V}$		0.75		V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 3.5\ \text{A}$		7.5		nC
Gate-Source Charge	Q_{gs}			0.6		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS} = 15\ \text{V}, V_{GS} = 0\ \text{V},$ $= 1\ \text{MHz}$	f	720		pF
Output Capacitance	C_{oss}			165		
Reverse Transfer Capacitance	C_{rss}			60		
Turn-On Delay Time	$t_{d(on)}$			8		
Rise Time	t_r	$V_{DD} = 10\ \text{V}, R_L = 15\ \Omega, I_D = 1\ \text{A},$ $V_{GEN} = 4.5\ \text{V}$		24		ns
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall Time	t_f			10		

Notes

- Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

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