CPM3-1200-0013A

V_{DS}	1200 V
$I_{D\ @\ 25^{\circ}C}$	149 A
$R_{DS(on)}$	13 mΩ

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enhancement Mode

Features

- C3M SiC MOSFET technlogy
- High Blocking Voltage with Low $R_{DS(on)}$
- Easy to parallel and simple to drive
- Resistant to Latch-up
- High Gate Resistance for Drives

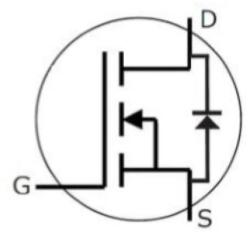
Benefits

- Higher System Efficiency
- Low Conduction Losses over Temperature
- Reduced Cooling Requirements
- Increased System Switching Frequency

Applications

- Automotive drive-train
- Motor drives
- Solid State Circuit Braker
- Resonant topologies

Inner Circuit



(G) Gate
(D) Drain
(S) Source

Part Number	Die Size (mm)
CPM3-1200-0013A	Please contact your sales representative to get the detailed information about die layout and dimensions.

Maximum Ratings

Symbol	Parameter		Value	Unit
V_{DSmax}	Drain - Source Voltage, $T_{vj} \geq -55\ ^{\circ}C$		1200	V
$V_{GSmax,\ AC}$ [1]	Max Transient Gate - Source Voltage		-8/+19	V
I_D [2]	Continuous Drain Current, t_p limited by T_{vjmax}, V_{GS} = 15V, assumes $R_{th(j-c)}$ < 0.28 K/W	$T_C = 25\ ^{\circ}C$	149	A
		$T_C = 100\ ^{\circ}C$	102	
$I_{D(pulse)}$ [2]	Pulsed Drain Current, t_p limited by T_{vjmax}		300	A
T_{VJ} , T_{stg} [2]	Virtual Junction and Storage Temperature		-55 to +175	˚C
T_{Proc}	Maximum Processing Temperature, in non-reactive ambient environment		325	˚C

[1] Recommended turn off / turn on gate voltage V_{GS} -4...0/+15V
[2] Verified by design

All parameters 100% tested at room temperature. Non-room temperature parameters are validated by design and statistical correlation.
Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for an extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA, T_{VJ} = 25ºC	
		1200			V	V_{GS} = 0 V, I_D = 100 μA T_{VJ} = -55ºC	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 27.9 mA, T_{VJ} = 25ºC	Fig. 11
			2.0		V	V_{DS} = V_{GS}, I_D = 27.9 mA, T_{VJ} = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	40	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance	9	13	17	mΩ	V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 25ºC	Fig. 4, 5, 6
			21			V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 175ºC	
g_{fs}	Transconductance		71		S	V_{DS}= 20 V, I_{DS}= 100 A, T_{VJ} = 25ºC	Fig. 7
			72			V_{DS}= 20 V, I_{DS}= 100 A, T_{VJ} = 175ºC	
C_{iss}	Input Capacitance		7560		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		284				
C_{rss}	Reverse Transfer Capacitance		18				
E_{oss}	C_{oss} Stored Energy		161		μJ		Fig. 16
$R_{G(int)}$	Internal Gate Resistance		6.7		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		77		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_{DS} = 100 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		95				
Q_g	Total Gate Charge		260				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.6		V	V_{GS} = -4 V, I_{SD} = 50 A, T_{VJ} = 25 °C	Fig. 8, 9, 10
		4.2		V	V_{GS} = -4 V, I_{SD} = 50 A, T_{VJ} = 175 °C	
t_{rr}	Reverse Recover time	43		ns	V_{GS} = -4 V, I_F = 100 A, V_R = 800 V dif/dt = 3000 A/μs, T_{VJ} = 175 °C	
Q_{rr}	Reverse Recovery Charge	1800		nC		
I_{rrm}	Peak Reverse Recovery Current	65		A		

Note: When using SiC Body Diode the maximum recommended V_{GS} = -4V

Typical Performance

All the graphs are based on the TO-247-4L (which has higher thermal resistance than most packages used with topside sinter/solder)

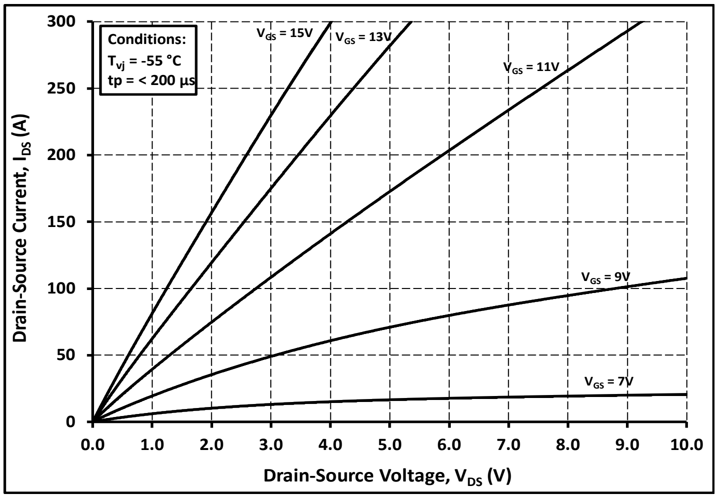


Figure 1. Output Characteristics T_{VJ} = -55 ºC

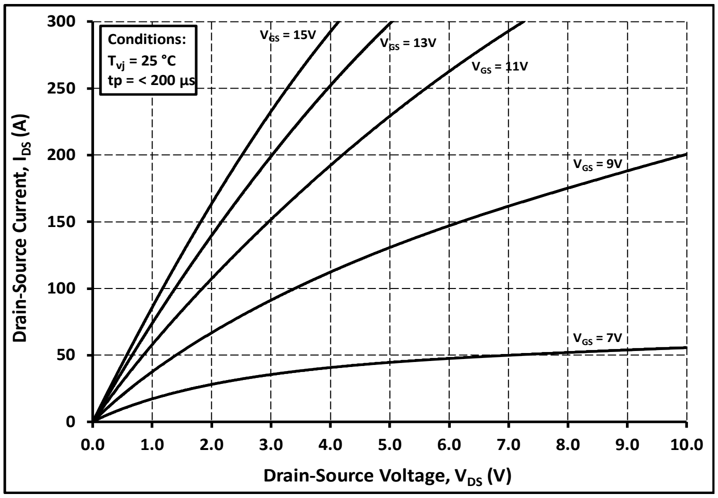


Figure 2. Output Characteristics T_{VJ} = 25 ºC

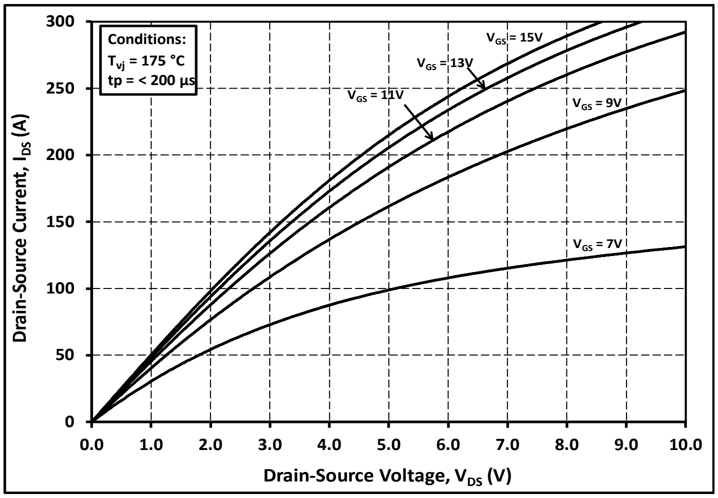


Figure 3. Output Characteristics T_{VJ} = 175 ºC

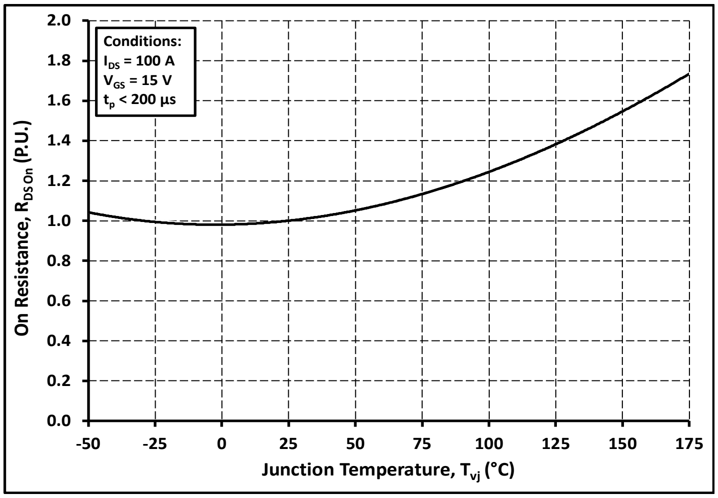


Figure 4. Normalized On-Resistance vs. Temperature

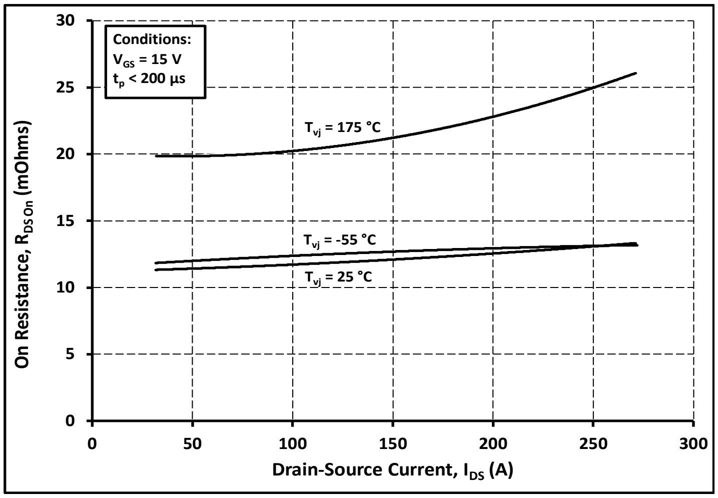


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

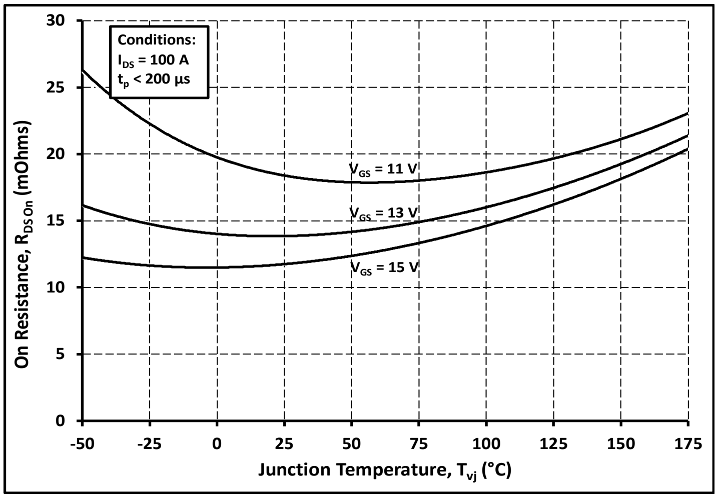


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

All the graphs are based on the TO-247-4L (which has higher thermal resistance than most packages used with topside sinter/solder)

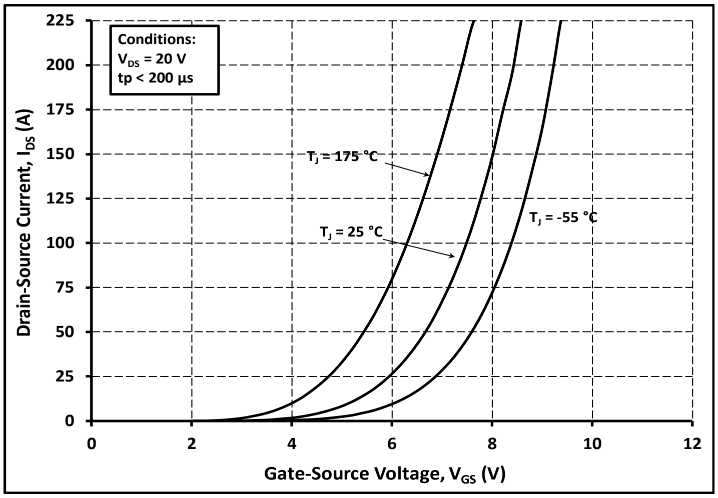


Figure 7. Transfer Characteristic for Various Junction Temperatures

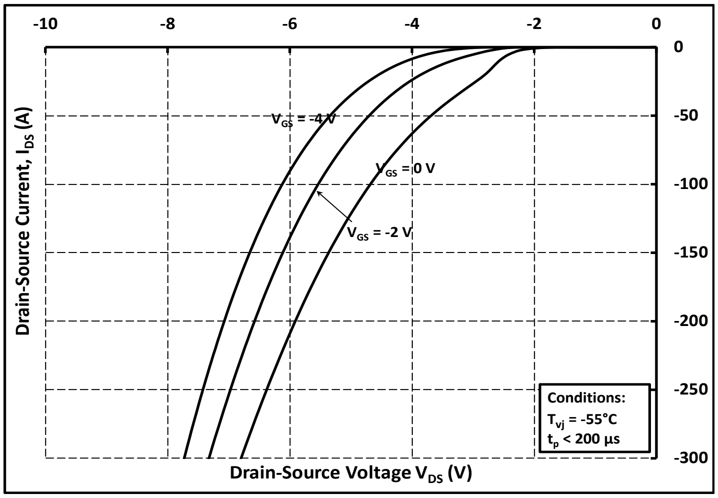


Figure 8. Body Diode Characteristic at -55 °C

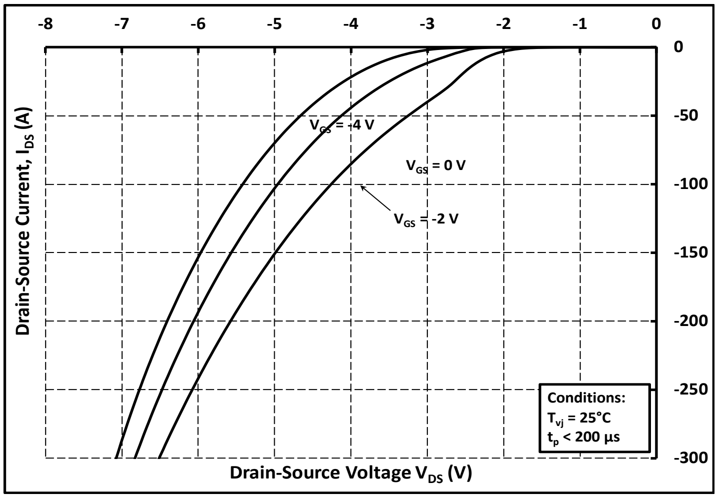


Figure 9. Body Diode Characteristic at 25 °C

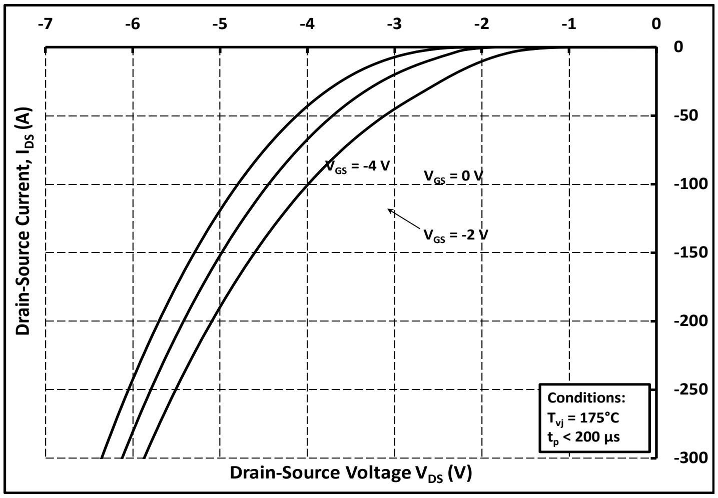


Figure 10. Body Diode Characteristic at 175 °C

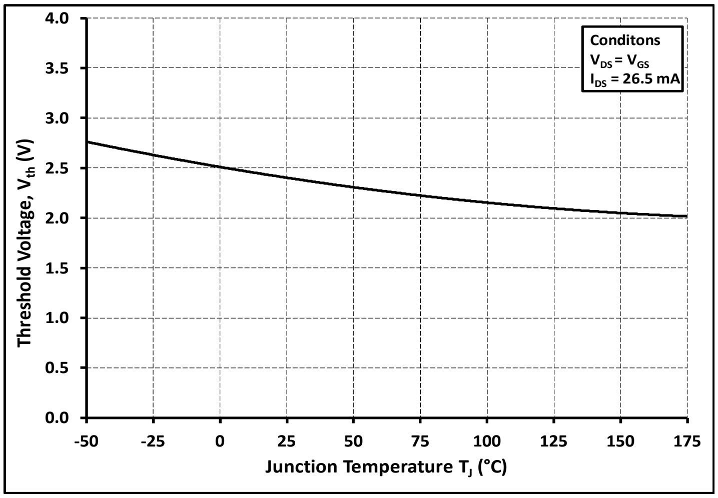


Figure 11. Threshold Voltage vs. Temperature

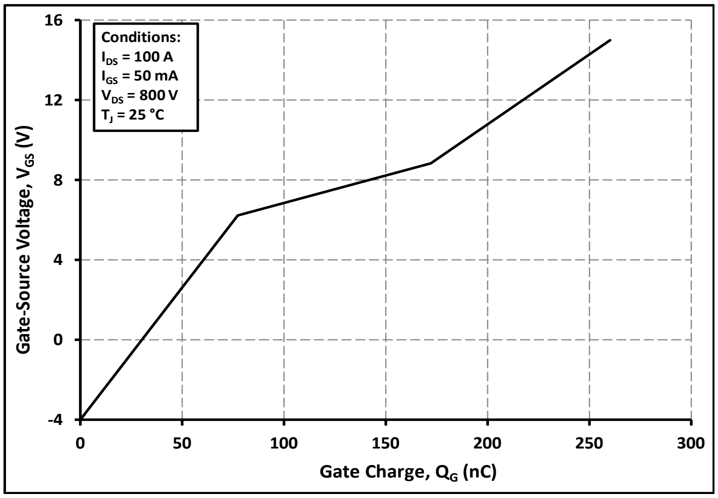


Figure 12. Gate Charge Characteristics

Typical Performance

All the graphs are based on the TO-247-4L (which has higher thermal resistance than most packages used with topside sinter/solder)

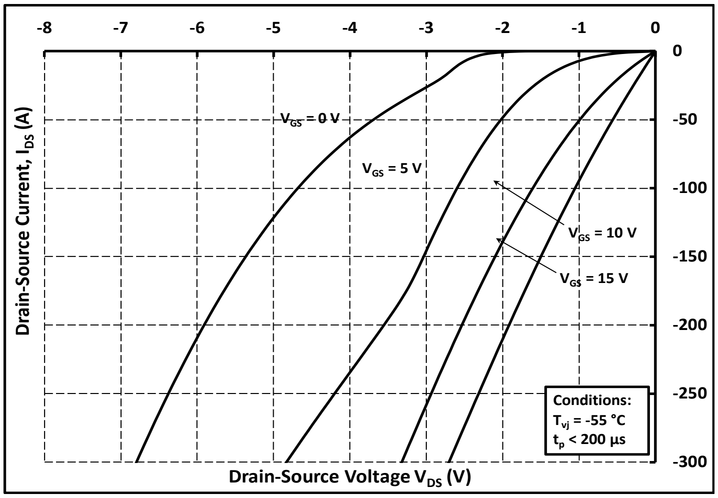


Figure 13. 3rd Quadrant Characteristic at -55 °C

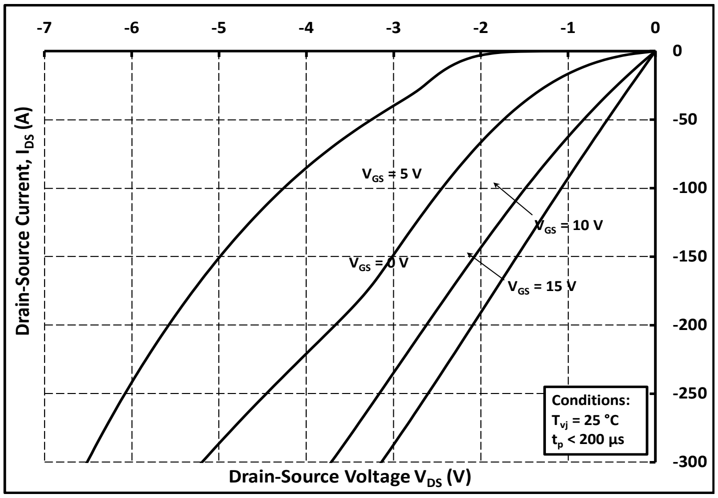


Figure 14. 3rd Quadrant Characteristic at 25 °C

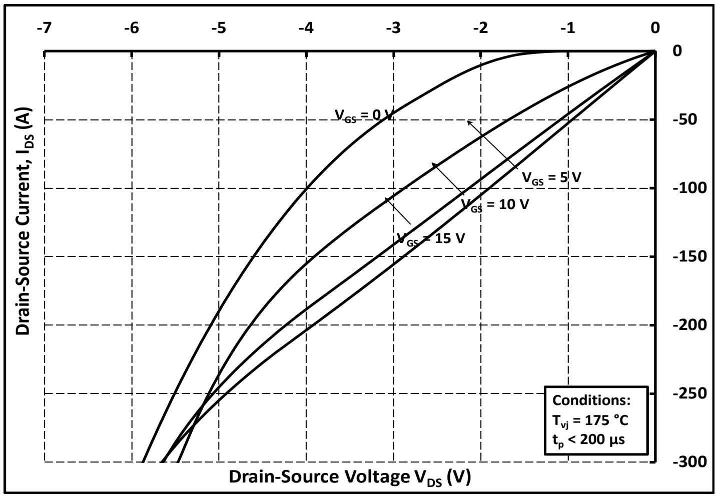


Figure 15. 3rd Quadrant Characteristic at 175 °C

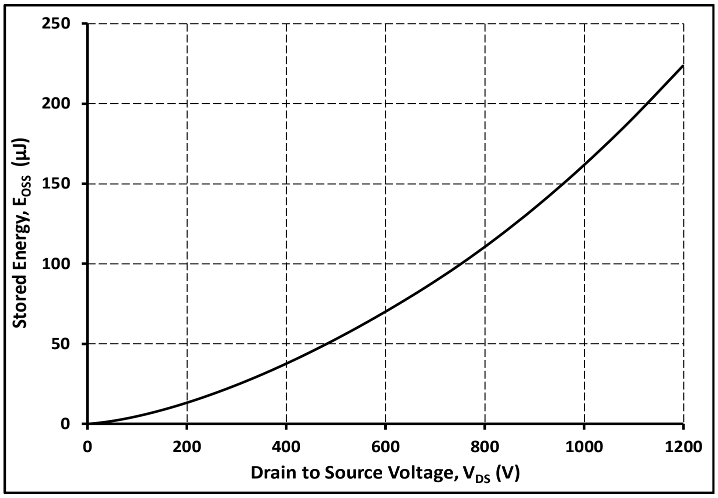


Figure 16. Output Capacitor Stored Energy

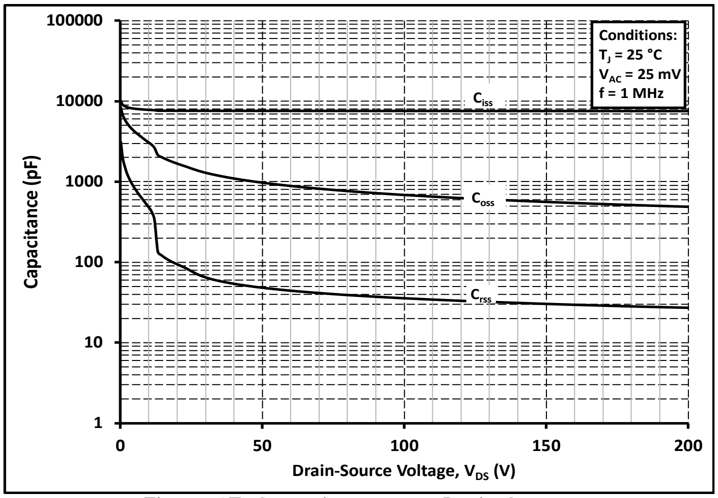


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

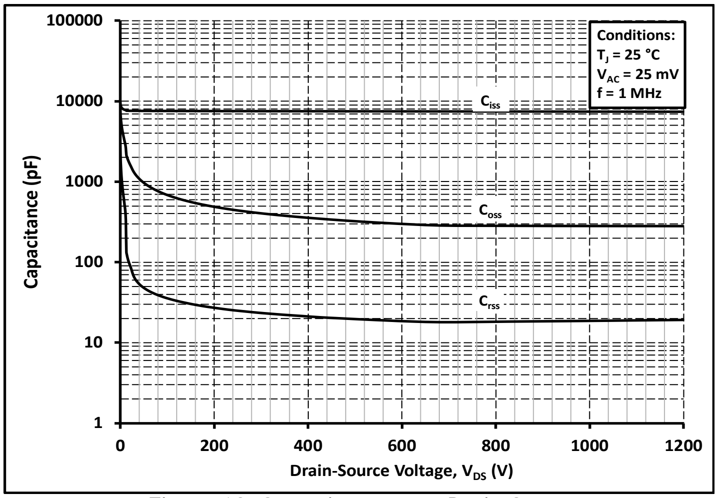


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Revision History

Revision Number	Date of Change	Brief Summary
-	04/02/2019	Initial Release
1	12/4/2019	• Removed test conditions and note section from the Maximum Ratings Table • Updated description for all the parameters in the Maximum Ratings Table • Updated footnotes • Temperature note removed and embedded into every test condition • Updated test conditions for gate threshold voltage, drain-source on-state resistance, transconductance, gate to source charge, gate to drain charge, total gate charge, diode forward voltage, reverse recovery time, reverse recovery charge and peak reverse recovery current • Updated typical values for continuous drain current, zero gate voltage drain current, gate-source leakage current, drain-source on-state resistance, transconductance, input capacitance, reverse transfer capacitance, Coss stored energy, gate too source charge, gate to drain charge, total gate charge, reverse recovery time and reverse recovery charge • All junction temperatures changed to virtual junction temperatures
2	02/24/2020	• Footnotes updated • Mechanical parameters corrected • All graphs updated to reflect the most recent test data

Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **SiC MOSFET Isolated Gate Driver reference design: www.wolfspeed.com/power/Tools-and-Support**
- **Application Considerations for Silicon-Carbide MOSFETs: www.wolfspeed.com/power/Tools-and-Support**

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