CMOS Voltage Converter – SiS7660

Switched-Capacitor Charge-Pump Voltage Converter IC in bare die form

Rev 1.0
20/07/20

Description

The SiS7660 converts a +1.5V to +10V supply into a corresponding -1.5V to -10V output. Operation is simple requiring x2 capacitors for charge-pump & charge-reservoir function. The SiS7660 can also function as a voltage doubler, generating output voltages up to +18.6V from a +10V input.

Oscillator, series regulator & logic control circuitry are integrated along with x4 MOS switches. The oscillator, when unloaded, oscillates at a nominal 10kHz with a 5V input supply. Oscillator frequency can be lowered by adding an external capacitor to the "OSC" terminal, or overdriven via an external clock. Tying the "LV" pin to GND bypasses the regulator to improve low voltage operation. At medium to high voltages (+3.5V to +10V) the LV pin is left floating to prevent device latch-up.

Features:

- Conversion of +5V Logic Supply to -5V
- Simple voltage multiplication ($V_{OUT} = (-) nV_{IN}$)
- Latch-up free via internal logic bias sense
- Typical open-circuit voltage conversion efficiency 99.9%
- Typical power efficiency 98%
- Wide Operating Voltage Range 1.5V to 10.0V
- Requires only x2 non-critical capacitors
- Direct replacement for industry standard ICL7660
- Full military temperature range.

Ordering Information

The following part suffixes apply:

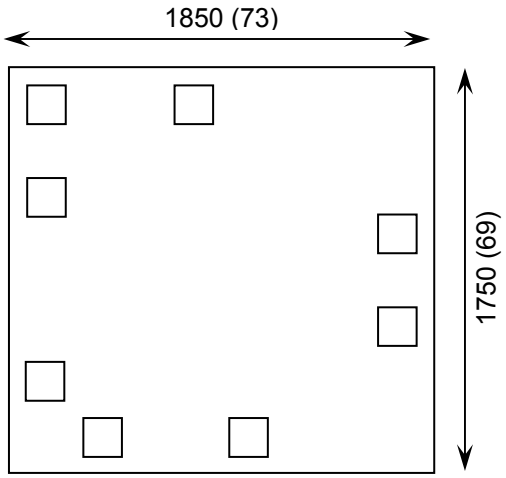
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 280µm(11 Mils) – On request
- In Metal or Ceramic package – On request

Mechanical Specification

Die Size (Unsawn)	1850 x 1750 73 x 69	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	280 (±20) 11 (±0.8)	µm mils
Top Metal Composition	Al 1%Si 1.4µm	
Back Metal Composition	N/A – Bare Si	

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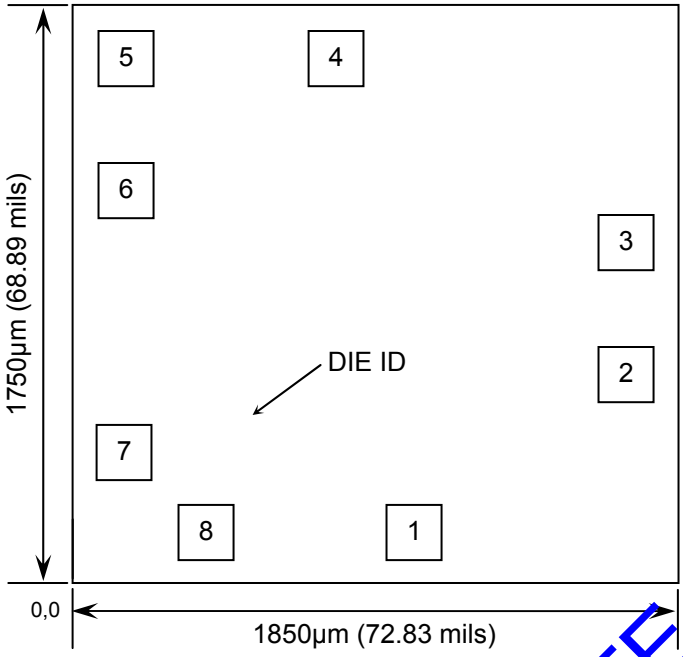
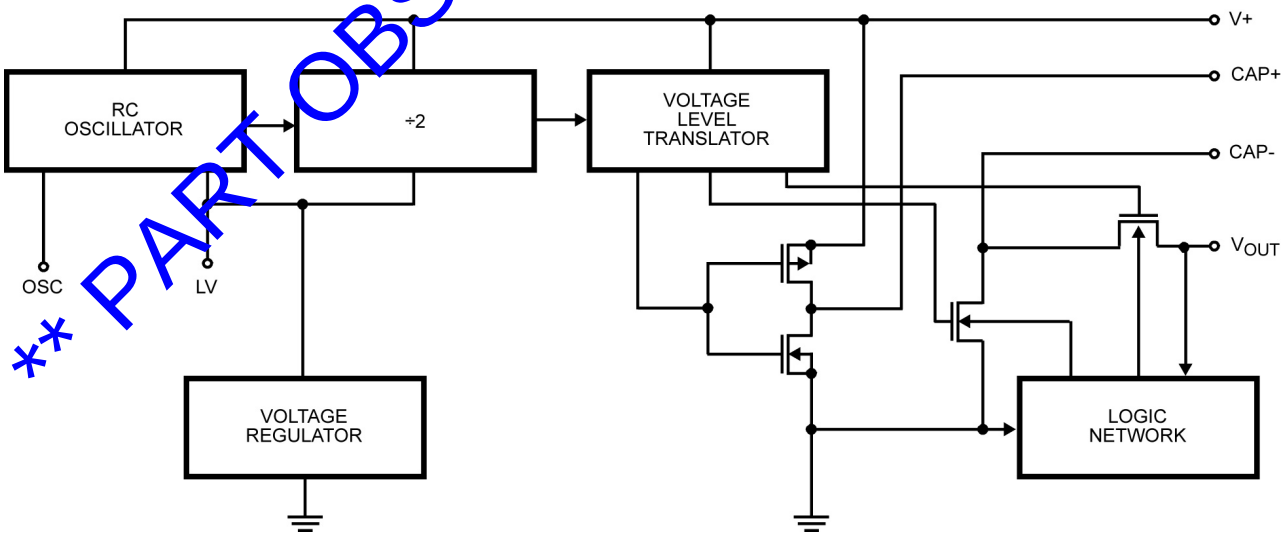
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	NC	1019	134
2	CAP +	1649	507.5
3	GND	1649	1038
4	CAP -	832	1549
5	V_{OUT}	101	1549
6	LV	101	338
7	OSC	101	1188
8	V+	253	134
CONNECT CHIP BACK TO V+ OR FLOAT			

Block Diagram



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Absolute Maximum Ratings[1] T_A = 25°C unless otherwise stated

PARAMETER	SYMBOL		VALUE	UNIT
Supply Voltage (V+ to GND or GND to V_{OUT})	V_S		+10.5	V
LV and OSC Input Voltage[2]	V_{IN}	V+ <5.5V	-0.3V to (V+ +0.3V)	V
		V+ >5.5V	(V+ -5.5V) to (V+ +0.3V)	
Current into LV[2]	I_{IN}	V+ >3.5V	20	µA
Output Short-Circuit Duration ($V_S \leq 5.5V$)	-		Continuous	
Operating Junction Temperature Range	T_J		-55 to 125	°C
Storage Temperature	T_{STG}		-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Connecting any input terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up".

Electrical Characteristics, T_A = 25°C, V+ = 5V, C_{OSC} = 0, unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_+	$R_L = \infty$	-	170	500	µA
Supply Voltage Range	V_{L+}	-55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV to GND	1.5	-	3.5	V
		-55°C ≤ T_A ≤ +125°C, R_L = 10kΩ, LV open	3.0	-	10	V
Output Source Resistance	R_{OU}	I_{OUT} = 20mA	-	55	100	Ω
		I_{OUT} = 20mA, -0°C ≤ T_A ≤ +70°C	-	-	120	
		I_{OUT} = 20mA, -55°C ≤ T_A ≤ +125°C	-	-	150	
		V+ = 2V, I_{OUT} = 3mA, LV to GND, 0°C ≤ T_A ≤ +70°C	-	-	300	
		V+ = 2V, I_{OUT} = 3mA, LV to GND, -55°C ≤ T_A ≤ +125°C	-	-	400	
Oscillator Frequency	f_{OSC}	-	8	-	18	kHz
Power Efficiency	P_{EF}	R_L = 5kΩ	95	98	-	%
Voltage Conversion Efficiency	$V_{OUT\ EF}$	$R_L = \infty$	97	99.9	-	%
Oscillator Impedance	Z_{OSC}	V+ = 2V	-	1	-	MΩ
		V+ = 5V	-	100	-	kΩ

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Application Notes

The SiS7660 capacitive charge-pump circuit either inverts, splits or doubles the input voltage (see Typical Applications).

- For highest performance, low effective series resistance (ESR) capacitors should be used
- If using inverting mode with a supply voltage less than +3.5V, LV may be connected to GND. This bypasses the internal regulator circuitry for best performance in low voltage applications. When using the inverter mode with supply voltage above +3.5V, LV must be left open.
- Do not short circuit the output to V+ for supply voltages >5.5V for extended periods, transient conditions including start-up are OK.
- If the voltage supply driving the SiS7660 has a large source impedance (25Ω - 30Ω), a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
- User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar placed in parallel with C2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 3).

Typical Applications & Adjustment Circuitry

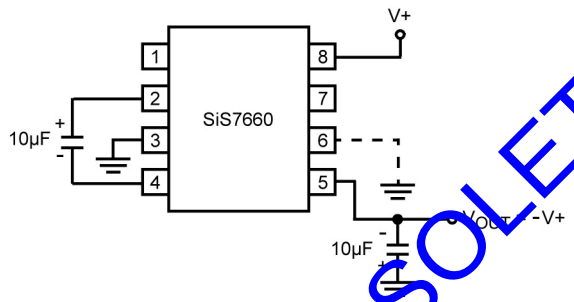

Figure 1 – Negative Voltage Converter

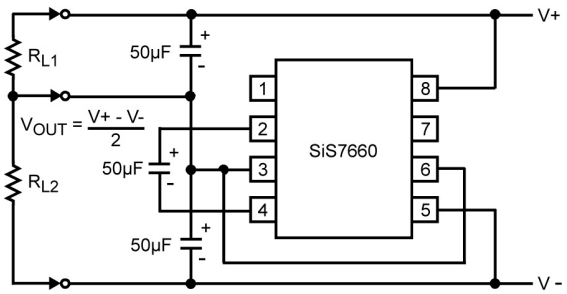

Figure 2 – Splitting supply Voltage in half

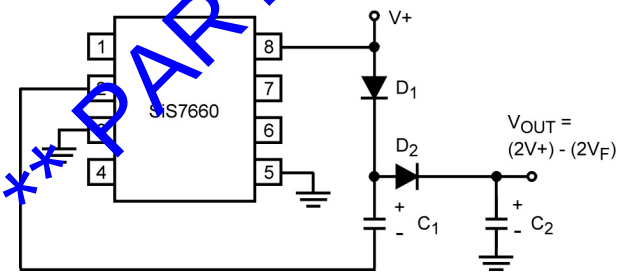

Figure 3 – Positive Voltage Doubler

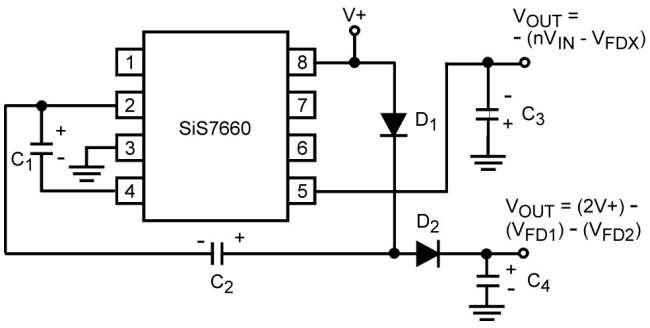

Figure 4 – Combined Negative Voltage Converter and Positive Doubler

Typical Applications & Adjustment Circuitry

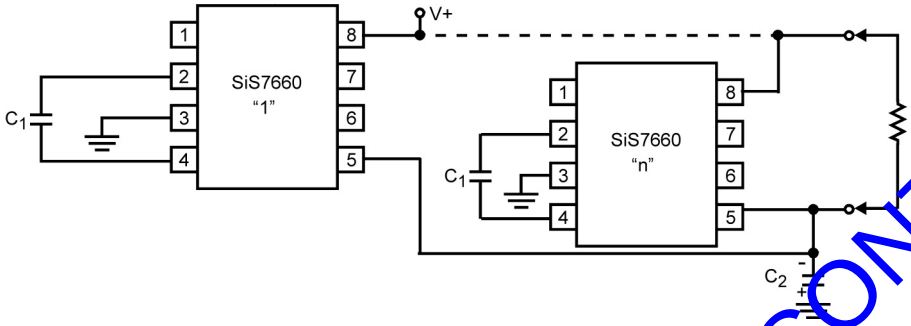

Figure 5 – Paralleling Devices

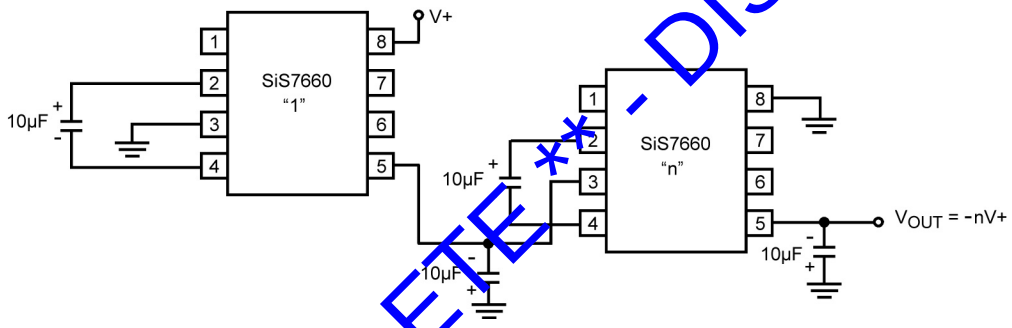

Figure 6 – Cascading devices for increased output voltage

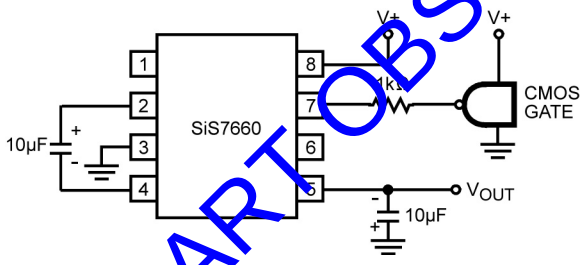

Figure 7 – External Clocking

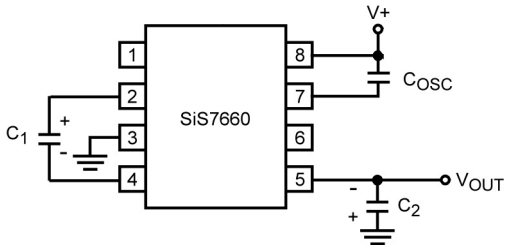

Figure 8 – Lowering Oscillator frequency