

Hex Schmitt Trigger Inverter in bare die form

Rev 1.0 17/02/2023

Description

The MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N-channel and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-} , show low variation with respect to temperature (typ. 0.0005 V/°C at V_{CC} = 10V), and hysteresis, V_{T+} - $V_{T-} \geq 0.2$ V_{CC} is guaranteed. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide supply voltage range: 3V to 150
- High noise immunity: 0.70 V_{cc} (type
- Low power TTL compatibuty.
 - 0.40 V_{CC} (type)
 - 0.20 V_{CC} (guaranteed)
- Hysteresis:
 - ~ 0.4 V_{co} (typ.)
 - o **⊘.2**0 V⊘ (guaranteed).

Ordering Information

The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please to

MM54C14

Die Dimensions in µm (mils)

*	1680	(66)	
	<u> </u>		1070 (42)

Supply Formats:

- Defaut Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

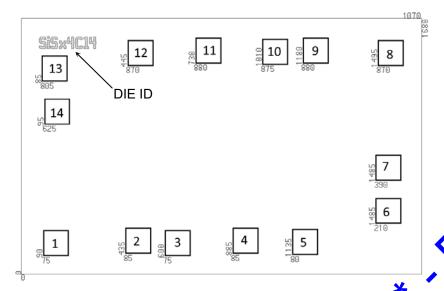
Die Size (Unsawn)	1680 x 1070 66.14 x 42.13	µm mils	
Minimum Bond Pad Size	105 x 105 4.713 x 4.13	μm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Al 1%Si 1.1μm		
Back Metal Composition	etal Composition N/A – Bare Si		





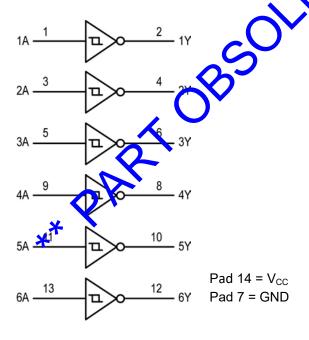
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Pad Layout and Functions



PAD	FUNCTION	COORDWATES (µm			
ו אט	1011011011	Х	Υ		
1	1A	90	75		
2	1Y	435	85		
3	2A	600	75		
4	21	885	85		
5	3A	1135	80		
6	31	1485	210		
70	GND	1485	390		
8	4Y	1495	870		
	4A	1180	880		
10	5Y	1010	875		
11	5A	730	880		
12	6Y	445	870		
13	6A	85	805		
14	V _{CC}	95	625		
CONNECT CHIP BACK TO V _{CC}					

Logic Diagram



Function Table

INPUT A	OUTPUT Y
L	Н
Н	L





Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT	
Voltage at any input pin	V _{IN}	-0.3 to V _{CC} + 0.3	N. T.	
Voltage at any output pin	V _{OUT}	-0.3 to V _{CC} + 0.3		
Operating V _{CC} range	V _{CC}	3 to 15	V	
Absolute maximum V _{CC}	V _{CC(MAX)}	18	V	
Maximum Power Dissipation ²	P _D	700	mW	
Operating Temperature Range	T _A	-40 to +85	°C	
Storage Temperature Range	T _{STG}	-65 to +150	°C	

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

DC Electrical Characteristics T_A = -40 to +85°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Positive Going Threshold Voltage		$V_{CC} = 5V$	3.0	3.6	4.3	V
	V _{T+}	V _{CC} = 10V	6.0	6.8	8.6	V
		V _{CC} = 15V	9.0	10.0	12.9	V
		$V_{CC} = 5V$	0.7	1.4	2.0	V
Negative Going Threshold Voltage	V _T -	V _{CC} = 10V	1.4	3.2	4.0	V
	\bigcirc	V _{CC} = 15V	2.1	5.0	6.0	V
C		$V_{CC} = 5V$	1.0	2.2	3.6	V
Hysteresis	V _{T+} - V _{T-}	V _{CC} = 10V	2.0	3.6	7.2	V
		V _{CC} = 15V	3.0	5.0	10.8	V
Logical "1" Output Voltage	V	$V_{CC} = 5V, I_{O} = -10\mu A$	4.5	-	-	V
Logical 1 Output Voltage	V _{OUT(1)}	$V_{CC} = 10V, I_{O} = -10\mu A$	9.0	-	-	V
Logical "0" Output Voltage	V _{OUT(0)}	$V_{CC} = 5V, I_{O} = 10\mu A$	-	-	0.5	V
Logical o Output voltage		$V_{CC} = 10V, I_{O} = 10\mu A$	-	-	1.0	V
Logical "1" Input Current	I _{IN(1)}	$V_{CC} = 15V, V_{IN} = 15V$	-	0.005	1.0	μA
Logical "C" Piput Current	I _{IN(0)}	V_{CC} = 15V, V_{IN} = 0V	-1.0	-0.005	-	μA
Supply Current	I _{CC}	$V_{CC} = 15V, V_{IN} = 0V/15V$	-	0.05	15	μA
*		$V_{CC} = 5V, V_{IN} = 2.5V$	-	20	-	μA
Supply Current ³	I _{CC}	$V_{CC} = 10V, V_{IN} = 5V$	-	200	-	μA
		$V_{CC} = 15V, V_{IN} = 7.5V$	-	600	-	μA

^{3.} Only one of the six inputs is at $1\!\!/_{\!2}\,V_{\text{CC}};$ the others are either at V_{CC} or GND.



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DC Electrical Characteristics $T_A = -40$ to +85°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
CMOS/LPTTL INTERFACE							
Logical "1" Input Voltage	V _{IN(1)}	$V_{CC} = 5V$	4.3	-		V	
Logical "0" Input Voltage	V _{IN(0)}	$V_{CC} = 5V$	-	-	0.7	V	
Logical "1" Output Voltage	V _{OUT(1)}	V _{CC} = 4.75V, I _O = -360μA	2.4	1	-	V	
Logical "0" Output Voltage	V _{OUT(0)}	$V_{CC} = 4.75V$, $I_{O} = 360\mu A$	-	-	0.4	V	
OUTPUT DRIVE CURRENT T _A = 25°C	OUTPUT DRIVE CURRENT T _A = 25°C						
Output Source Current	I _{SOURCE}	$V_{CC} = 5V$, $V_{OUT} = 0V$	-1. 5	-3.3	-	mA	
(P-Channel)	SOURCE	$V_{CC} = 10V, V_{OUT} = V$	-8.0	-15	-	mA	
Output Source Current	I _{SINK}	$V_{CC} = 5V, V_{OUT} = V_{CT}$	1.75	3.6	-	mA	
(N-Channel)	ISINK	$V_{CC} = 10V_{CC} = V_{CC}$	8.0	16	-	mA	
DYNAMIC ELECTRICAL CHARACTER	STICS ⁴ T _A = 25	°C, C _L = 50 F upless oth	erwise s	stated			
Propagation Delay	t _{PD0,}	V _{2C} = 5V	-	220	400	ns	
from Input to Output	t _{PD1}	V _{CC} = 10V	-	80	200	ns	
Input Capacitance	C _{IN}	Any Input	-	5.0	-	pF	
Power Dissipation Capacitance ⁵	C _{PD}	Per Gate	-	20	-	pF	

^{4.} Not production tested in die form, characterized by chip design

Typical Characteristics

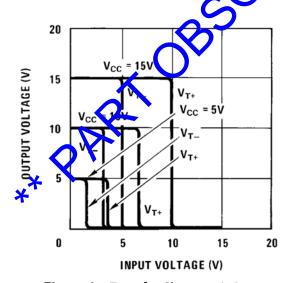


Figure 1 – Transfer Characteristics

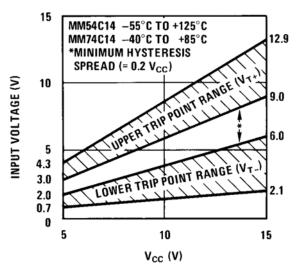


Figure 2 – Guaranteed Trip Point Range

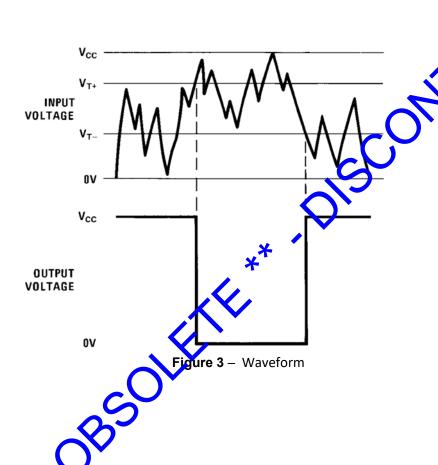


^{5.} Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.



Typical Characteristics continued

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