



Linear Voltage Regulator – LM317L

Positive Adjustable 100mA output Voltage Regulator in bare die form

Rev 1.0
05/09/18

Description

The LM317L is a wide V_{IN} adjustable 3-terminal low power voltage regulator equipped with internal limiting + thermal shutdown features for overload immunity. Output voltage is set by two external resistors. Additional to standard regulator function, the device can be used as a simple adjustable switching regulator; a programmable output regulator; or by connecting a fixed resistor between adjustment pin and output, can be used as a precision current regulator. A shutdown mechanism can be introduced by clamping the adjust terminal to ground which programs output to 1.2V where most loads draw little current.

Features:

- Adjustable output between 1.2V - 37V
- Internal short circuit current limit
- Internal thermal overload protection
- Output transistor Safe Area Compensation
- Floating operation for high voltage applications
- 0.01% Line, 0.1% Load regulation
- Negative Voltage complement is LM337

Ordering Information

The following part suffixes apply:

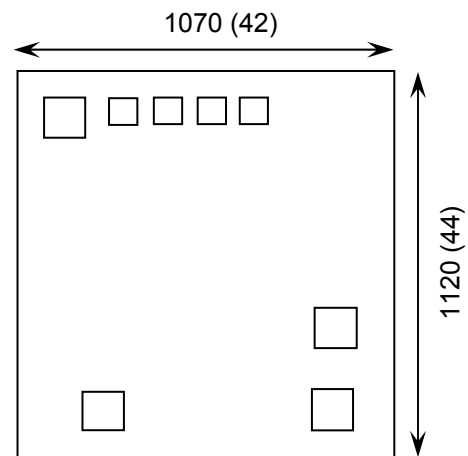
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in μm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Tape & Reel – On request
- In Metal or Ceramic package – On request

Mechanical Specification

Die Size (Unsawn)	1070 x 1120 42 x 44	μm mils
Minimum Bond Pad Size	90 x 90 3.54 x 3.54	μm mils
Die Thickness	350 (± 20) 13.78 (± 0.79)	μm mils
Top Metal Composition	Al 1%Si 2.2 μm	
Back Metal Composition	Si	



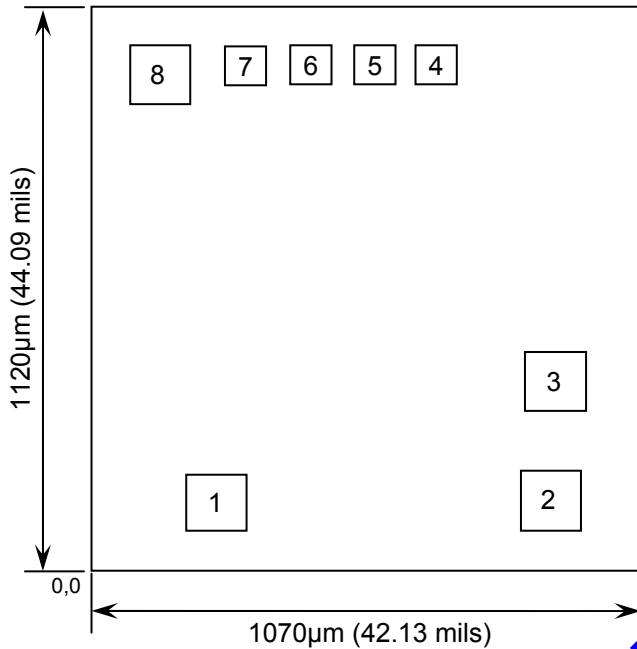


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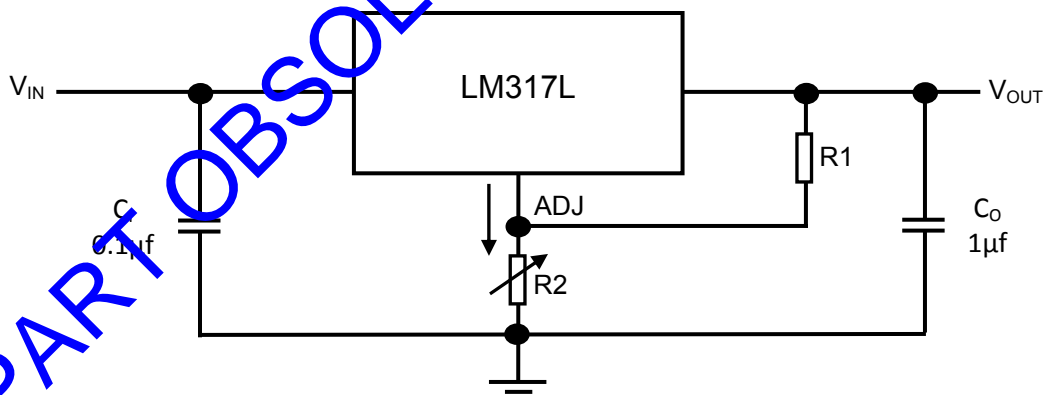
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	V _{OUT}	0.217	0.070
2	V _{OUT}	0.910	0.070
3	V _{IN}	0.890	0.328
4	NC	0.645	0.989
5	NC	0.505	0.989
6	NC	0.365	0.989
7	NC	0.225	0.989
8	ADJUST	0.065	0.965

NC = NO CONNECT
CONNECT CHIP BACK TO V_{OUT}

Typical Application



1.2V–25V Adjustable Regulator

$$V_{OUT} = 1.25V \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} * R_2$$

I_{ADJ} tolerance <100µA

C_i is required if the regulator is located an appreciable distance from power supply filter. C_o is not required for stability; however it does improve transient response. For optimum stability and transient response locate C_i C_o as close as possible to the regulator.





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
Input–Output Voltage differential	$V_{IN} - V_{OUT}$	40	V
Power Dissipation	P_D	Internally Limited	
Operating Junction Temperature	T_J	-40 to 125	°C
Storage Temperature	T_{STG}	-65 to 150	°C

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Output Voltage	V_{OUT}	1.25	37	V
Input–Output Voltage differential	$V_{IN} - V_{OUT}$	4	40	V
Output Current	I_{OUT}	10	100	mA
Operating Junction Temperature Range	T_J	-40 to 125		°C

DC Electrical Characteristics, $V_{IN} - V_{OUT} = 5V$, $I_{OUT} = 40mA$, $I_{MAX} = 100mA$, $T_J = -40^\circ C$ to $125^\circ C$ (unless noted otherwise)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	$3V \leq V_{IN} - V_{OUT} \leq 40V$, $5mA \leq I_{OUT} \leq I_{MAX}$, $P_D \leq 625mW$	1.20	1.25	1.30	V
Line Regulation ²	ΔV_{OUT}	$3V \leq V_{IN} - V_{OUT} \leq 40V$, $I_L \leq 20mA$, $T_J = 25^\circ C$	-	0.01	0.04	% / V_{OUT}
		$3V \leq V_{IN} - V_{OUT} \leq 40V$, $I_L \leq 20mA$	-	0.02	0.07	
Load Regulation ²	ΔV_{OUT}	$V_O = \leq 5V$, $10mA \leq I_{OUT} \leq I_{MAX}$, $T_J = 25^\circ C$	-	5	25	mV
		$V_O = \geq 5V$, $10mA \leq I_{OUT} \leq I_{MAX}$, $T_J = 25^\circ C$	-	0.1	0.5	% / V_{OUT}
		$V_O = \leq 5V$, $10mA \leq I_{OUT} \leq I_{MAX}$	-	20	70	mV
		$V_O = \geq 5V$, $10mA \leq I_{OUT} \leq I_{MAX}$	-	0.3	1.5	% / V_{OUT}
Thermal Regulation		20ms pulse, $T_J = 25^\circ C$	-	0.04	0.2	% / W
Adjustment Pin Current	I_{ADJ}		-	50	100	μA
Adjustment Pin Current Change	ΔI_{ADJ}	$2 \leq V_{IN} - V_{OUT} \leq 40V$, $5mA \leq I_L \leq I_{MAX}$, $P_D \leq 625mW$	-	0.2	5	μA
Temperature Stability	-	$T_{LOW} \leq T_J \leq T_{HIGH}$	-	0.65	-	%
Minimum Load Current	I_L	$ V_{IN} - V_{OUT} = 40V$	-	3.5	5	mA
		$3V \leq V_{IN} - V_{OUT} \leq 15V$	-	1.5	2.5	
Output Current Limit ³	I_{MAX}	$3V \leq V_{IN} - V_{OUT} \leq 13V$	100	200	300	mA
		$ V_{IN} - V_{OUT} = 40V$	25	50	150	mA

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

2. Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.





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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RMS Output Noise, % of V_{OUT}	eN	$10\text{ Hz} \leq f \leq 10\text{ kHz}$, $T_J = 25^{\circ}C$	-	0.003	-	%
Ripple Rejection Ratio	RR	$V_{OUT} = 10V$, $f = 120\text{ Hz}$, $C_{ADJ} = 0\mu F$	-	65	-	dB
		$V_{OUT} = 10V$, $f = 120\text{ Hz}$, $C_{ADJ} = 10\mu F$	66	80	-	
Long Term Stability	-	$T_A = 125^{\circ}C$, 1000 hrs	-	0.3	1	%
Thermal Resistance ³	$R\theta_{JC}$	$T_{LOW} \leq T_J \leq T_{HIGH}$	-	180	-	$^{\circ}C/W$

3. Assembled in TO-92 package. Die form performance is dependent on die attach, substrate choice & assembly method.

Typical Electrical Characteristics, $T_J = 25^{\circ}C$ (unless noted otherwise)

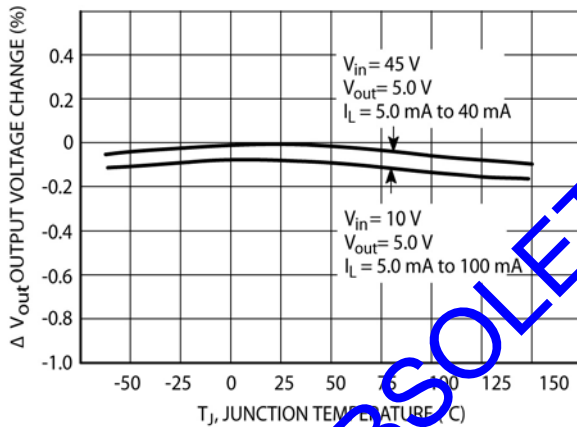


Figure 1 – Load Regulation

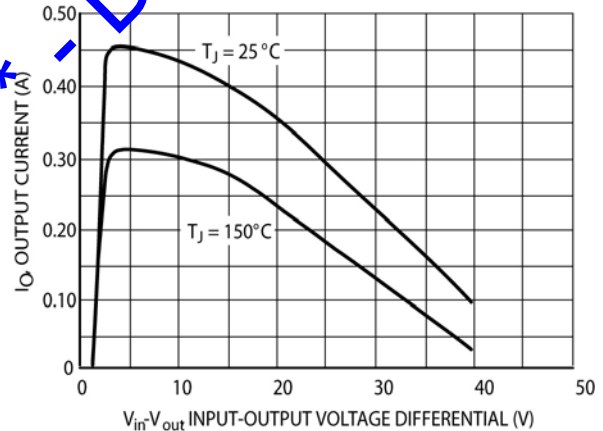


Figure 2 – Current Limit

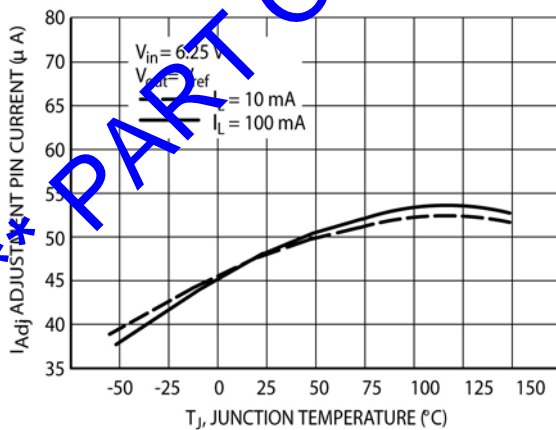


Figure 3 – Adjustment Pin Current

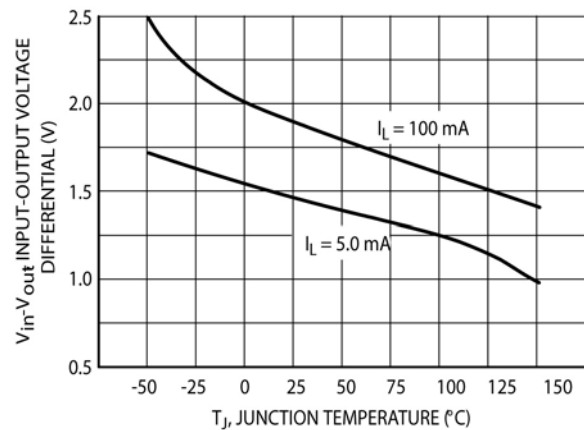


Figure 4 – Dropout Voltage





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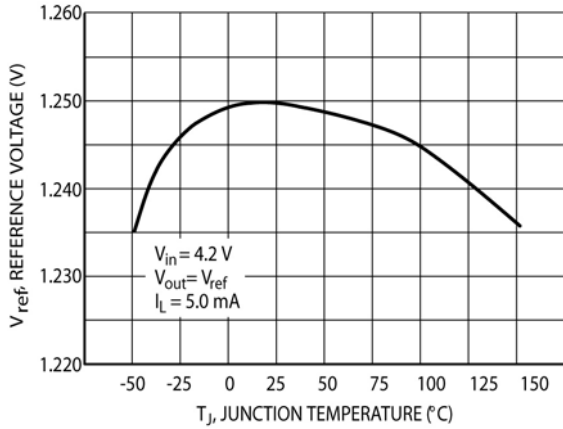


Figure 5 – Temperature Stability

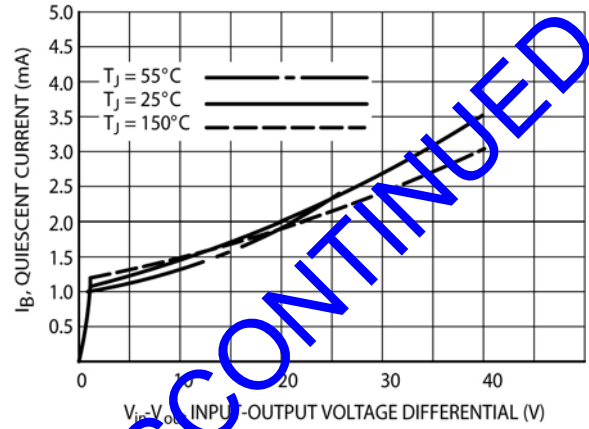


Figure 6 – Minimum Operating Current

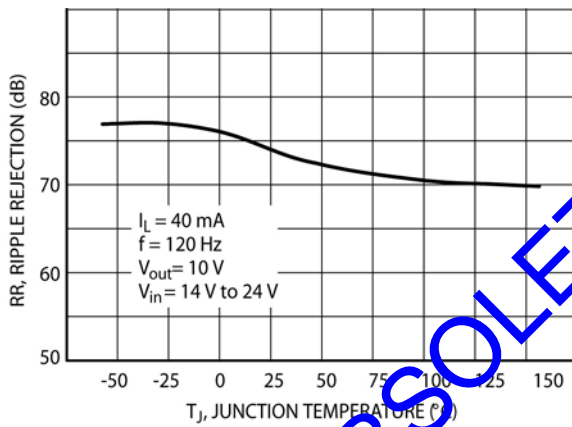


Figure 7 – Ripple Rejection

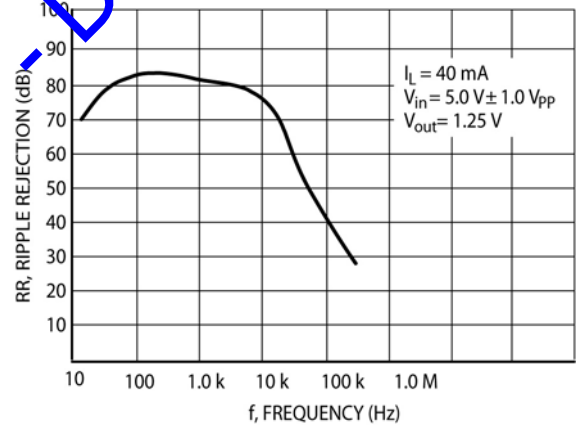


Figure 8 – Ripple Rejection versus Frequency

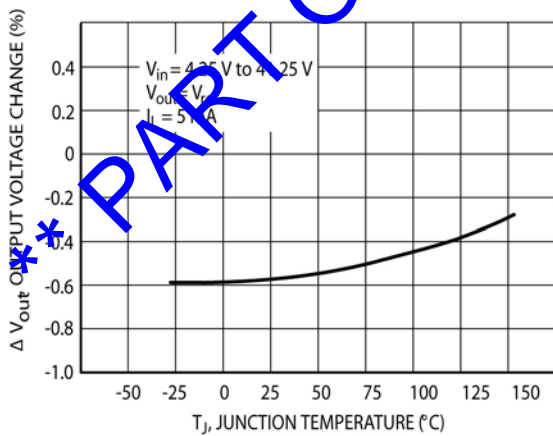


Figure 9 – Line Regulation

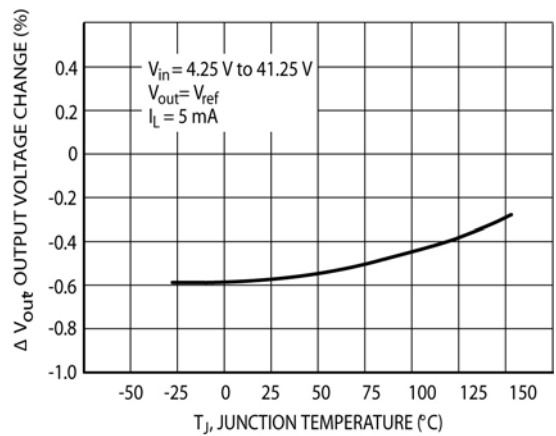


Figure 10 – Output Noise





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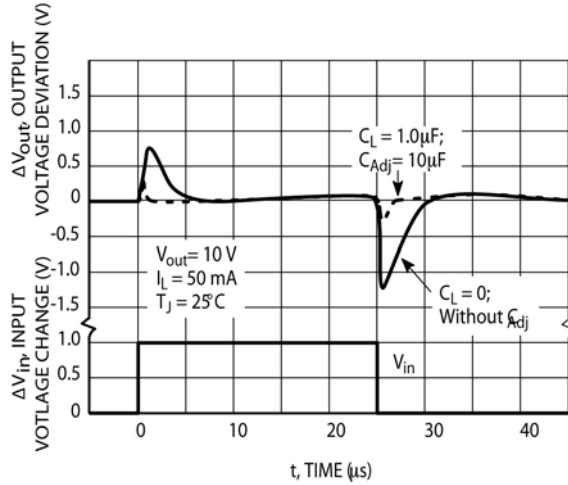


Figure 11– Line Transient Response

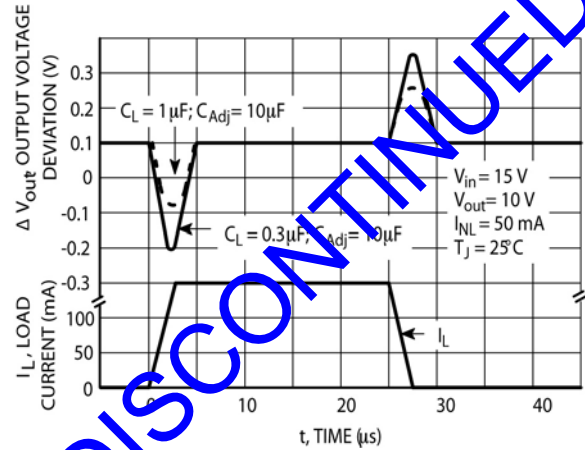


Figure 12– Load Transient Response

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