

Positive Adjustable 1.5A output Voltage Regulator in bare die form

Rev 1.0 03/03/18

Description

The LM317 is a wide V_{IN} adjustable 3-terminal voltage regulator with guaranteed 1.5A output current and equipped with internal limiting + thermal shutdown features for overload immunity. Output voltage is set by two external resistors. Additional to standard regulator function, the device can be used as a simple adjustable switching regulator; a programmable output regulator; or by connecting a fixed resistor between adjustment pin and output, can be used as a precision current regulator. A shutdown mechanism can be introduced by clamping the adjust terminal to ground which programs output to 1.2V where most loads draw little current.

Ordering Information

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection
 + MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual (spection (Space))
 + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality\bare-die-lot-qualification

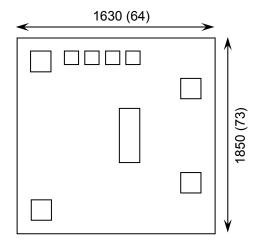
Supply Formats:

- Default Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Tape & Reel On request
- In Metal or Ceramic package On request

Features:

- Output current in excess of 1.5A
- Adjustable output between 1.2 37
- Internal short circuit current unit
- Internal thermal overlead protection
- Output transistor Safe-Area Compensation
- Floating operation on high voltage applications
- 0.01% Line & 0.1% Load Regulation
- Negative Voltage complement is LM337

Die Dimensions in µm (mils)



Mechanical Specification

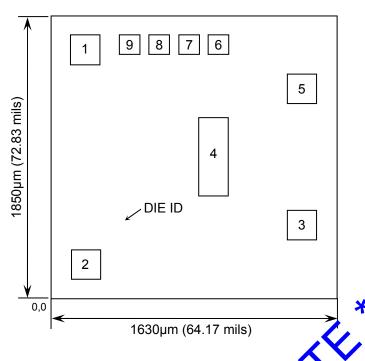
Die Size (Unsawn)	1630 x 1850 64 x 73	μm mils	
Minimum Bond Pad Size	140 x 140 5.51 x 5.51	μm mils	
Die Thickness	350 (±20) 13.78 (±0.79)		
Top Metal Composition	Al 1%Si 2.2μm		
Back Metal Composition	Ti/Ni/Ag 1.2 μm		





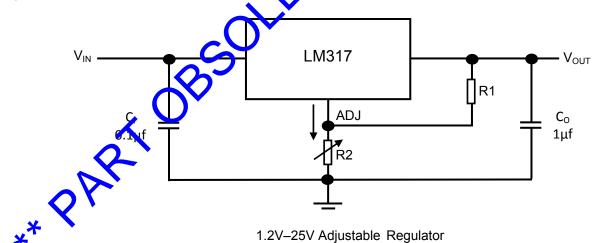
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Pad Layout and Functions



PAD	FUNCTION	COORDINA	1.400 0.331 0.773 0.714 1.400 1.402 0.641 1.715
IAD	TONCTION	Х	Y
1	V _{OUT}	0.013	1.637
2	ADJ	0.073	0.073
3	V _{OUT}	1.400	0.331
4	V _{IN} (x2 wird)	0.773	0.714
5	V _{OU} -	1.400	1.402
6	IAC.	0.641	1.715
_C	NC	0.512	1.715
9	NC	0.383	1.715
Э	NC	0.254	1.715
	NC = NO	CONNECT	
	CONNECT CH	IP BACK TO	Vout

Typical Application



 $V_{OUT} = 1.25V (1 + \frac{R2}{R1}) + I_{ADJ} * R2$

I_{ADJ} tolerance <100μA

 C_l is required if the regulator is located an appreciable distance from power supply filter. C_0 is not required for stability; however it does improve transient response. For optimum stability and transient response locate C_l C_0 as close as possible to the regulator.





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNI	
Input–Output Voltage differential	V _{IN} - V _{OUT}	40	V	
Power Dissipation	P _D	Internally Limited		
Operating Junction Temperature	T _J	150	C	
Storage Temperature	T _{STG}	-65 to 150	°C	

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN MAX	UNIT
Output Voltage	V _{OUT}	1 25 37	V
Input–Output Voltage differential	V _{IN} - V _{OUT}	4 1 40	V
Output Current	I _{out}	01 1.5	Α
Operating Junction Temperature Range	T _J	0 to 125	°C

DC Electrical Characteristics, V_{IN}-V_{OUT}=5V, I_{OUT}=0.5A, I_{MX} = 1.5A, T_J = 0°C to +125°C(unless noted otherwise)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	$3V \le V_{IN} - V_{OUT} \le 40V$, $10\text{mA} \le I_{OUT} \le I_{IN} \times V$	1.2	1.25	1.30	V
Line Regulation ²	ΔV_{OUT}	$3V \le V_{IN} - V_{OUT} \le 40V, T_J = 25^{\circ}C$	-	0.01	0.04	% / V _{OUT}
Line Regulation	4 0 0 0 0 0 0 0	$3V \le V_{II} - V_{OUT} \le 40V$		0.02	0.07	70 7 4 001
		$V_{IN} \le 5V,10$ $A \le I_{OUT} \le I_{MAX}, T_J = 25$ °C	-	5	25	mV
Load Regulation ²	ΔV_{OUT}	$V_N \ge 3V$, $OmA \le I_{OUT} \le I_{MAX}$, $T_J = 25$ °C	-	0.1	0.5	% / V _{OUT}
		$V_N \le V,10$ mA $\le I_{OUT} \le I_{MAX}$	-	20	70	mV
		$V_N \ge 5V,10\text{mA} \le I_{OUT} \le I_{MAX}$	-	0.3	1.5	% / V _{OUT}
Thermal Regulation		20ms pulse, T _J = 25°C	-	0.03	0.07	% / W
Adjustment Pin Current			-	50	100	μA
Adjustment Pin Current Chang	ΔI_{ADJ}	$2.5V \le V_{IN} - V_{OUT} \le 40V$, $10\text{mA} \le I_L \le I_{MAX}, P_D \le P_{MAX}$	-	0.2	5.0	μΑ
Temperature Stability	-	$T_{LOW} \le T_{J} \le T_{HIGH}$	-	1	-	%
Minimun Load Current	IL	V _{IN} -V _{OUT} = 40V	-	3.5	10	mA
Output Current		$ V_{IN} - V_{OUT} \le 15V, P \le 20W$	1.5	2.2	-	А
Limit ³	I _{MAX}	$ V_{IN} - V_{OUT} = 40V, P \le 20W, T_J = 25^{\circ}C$	0.15	0.40	-	

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

^{2.} Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.





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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
RMS Output Noise, % of V _{OUT}	eN	10 Hz ≤ f ≤ 10 kHz, T _J = 25°C	-	0.003	-	%
Ripple Rejection RR	$V_{OUT} = 10V, f = 120 \text{ Hz}, C_{ADJ} = 0\mu\text{F}$	-	65		dB	
	$V_{OUT} = 10V, f = 120 \text{ Hz}, C_{ADJ} = 10\mu\text{F}$	66	80		QB.	
Long Term Stability	-	T _A = 125°C, 1000 hrs	-	0.3	1	%
Thermal Resistance ³	Rθ _{JC}	$T_{LOW} \le T_{J} \le T_{HIGH}$	-	2	-	°C/W

^{3.} Assembled in TO-3 package. Die performance is dependent on die attach, substrate choi e & assembly method.

Typical Electrical Characteristics, TJ = 25°C (unless noted in wise)

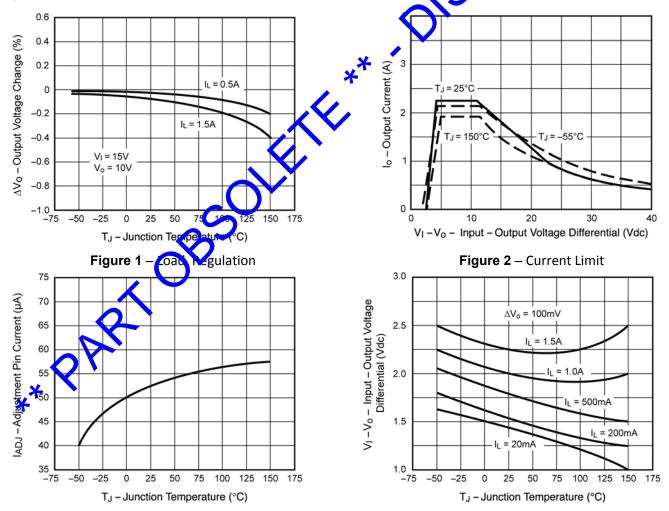


Figure 3 – Adjustment Pin Current

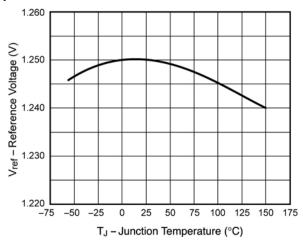
Figure 4 – Dropout Voltage





Typical Electrical Characteristics, T_J = 25°C (unless noted otherwise)

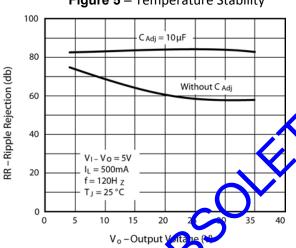
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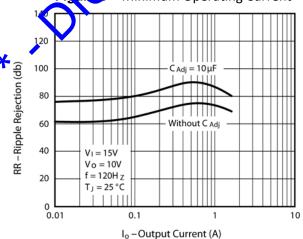


4.5 Io - Quiescent Current (mA) 4.0 3.5 3.0 2.5 2.0 1.5 1.0 0.5 Output Voltage Differential (Vdc)

Figure 5 – Temperature Stability

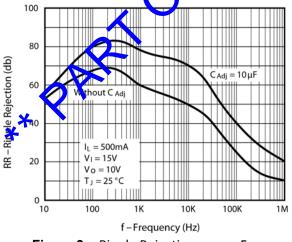
Figure 9 – Minimum Operating Current





ss Output Voltage Figure 7 - Ripple Reject

Figure 8 - Ripple Rejection versus Output Current



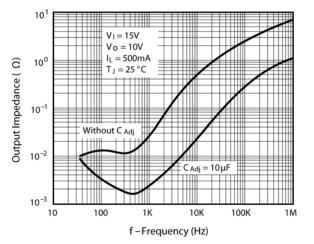


Figure 9 – Ripple Rejection versus Frequency

Figure 10 - Output Impedance





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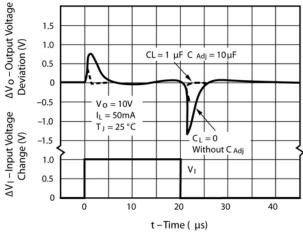
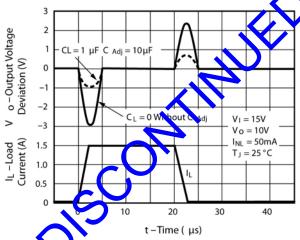
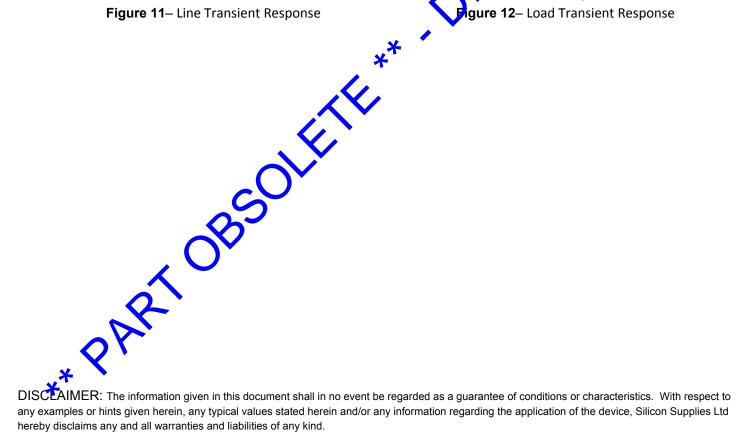


Figure 11- Line Transient Response



gure 12- Load Transient Response



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