CMOS High Voltage Logic – CD4093B

Quadruple 2-Input NAND Gate Logic IC with Schmitt-Trigger Inputs in bare die form

Rev 1.0
21/11/17

Description

The CD4093B Quad 2-Input NAND Gate is fabricated using a 3µm 15CMOS process. This device consists of x4 Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt trigger action on both inputs. The gate switches at different points for positive & negative-going signals. The difference between the positive (V_T+) & the negative voltage (V_T−) is defined as hysteresis voltage (V_H). Device hysteresis characteristics transform slowly changing input signals into sharply defined jitter-free output signals.

Features:

- High Input Voltage up to 20V
- Schmitt-trigger on each input
- No limit on input rise and fall times
- Noise immunity greater than 50%
- Drives x2 Low-Power TTL loads or x1 LSTTL load
- Symmetrical Sink & Source Currents
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

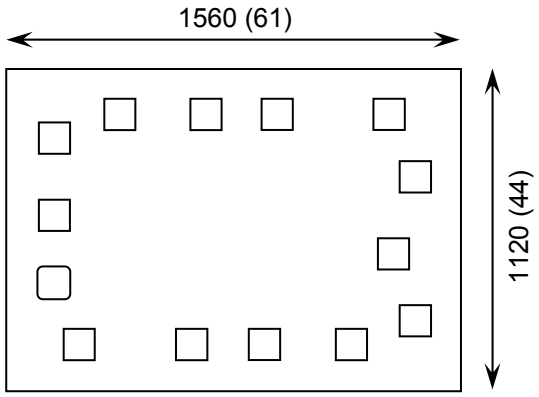
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1560 x 1120 61 x 44	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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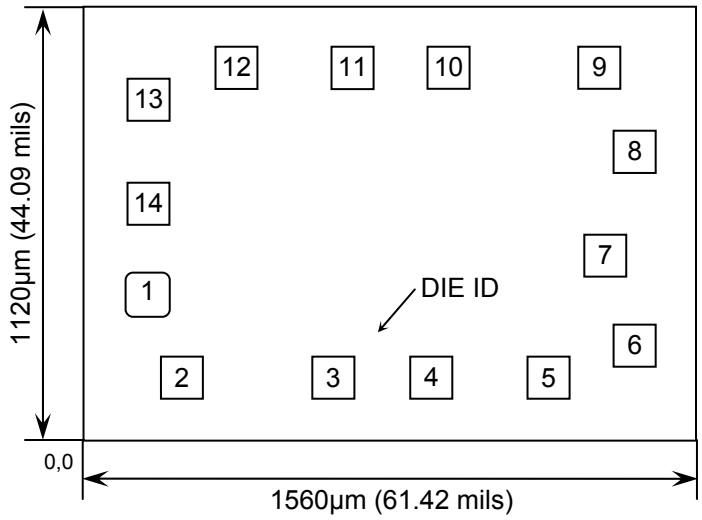
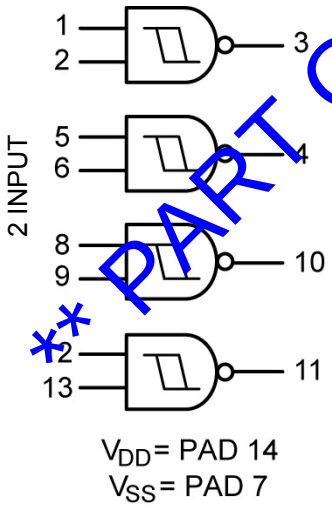
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A1	0.1135	0.3290
2	B1	0.2005	0.1130
3	Y1	0.5865	0.1130
4	Y2	0.8305	0.1130
5	A2	1.1235	0.1130
6	B2	1.3460	0.1975
7	V_{SS}	1.2765	0.4280
8	A3	1.3460	0.6910
9	B3	1.2595	0.9070
10	Y3	0.8735	0.9070
11	Y4	0.6295	0.9070
12	A4	0.3365	0.9070
13	B4	0.1140	0.8225
14	V_{DD}	0.1135	0.5595
CONNECT CHIP BACK TO V_{DD} OR FLOAT			

Logic Diagram



V_{DD} = PAD 14
V_{SS} = PAD 7

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High level (steady state)
L = Low level (steady state)

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input or Output Voltage (Referenced to V_{SS})	V_{IN}, V_{OUT}	-0.5 to V_{DD}+0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current or Output Current (per Pad)	I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air[2]	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3.0	18	V
DC Input Voltage, Output Voltage	V_{IN}, V_{OUT}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	5V	V_{IN} = V_{DD} or V_{SS}	4.95	4.95	4.95	V
		10V	V_{IN} = V_{DD} or V_{SS}	9.95	9.95	9.95	
		15V	V_{IN} = V_{DD} or V_{SS}	14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	V_{IN} = V_{DD}	0.05	0.05	0.05	V
		10V	V_{IN} = V_{DD}	0.05	0.05	0.05	
		15V	V_{IN} = V_{DD}	0.05	0.05	0.05	
Maximum Input Leakage Current	I_{IN}	18V	V_{IN} = V_{DD} or V_{SS}	±0.1	±0.1	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{DD}	5V	V_{IN} = V_{DD} or V_{SS} I_{OUT} = 0µA	1	30	30	µA
		10V		2	60	60	
		15V		4	20	120	
		20V		20	60	600	
Minimum Output Low (Sink) Current	I_{OL}	5V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	0.64	0.42	0.36	mA
		10V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.5V	1.6	1.1	0.9	
		15V	V_{IN} = V_{DD} or V_{SS} V_{OL} = 1.5V	4.2	2.8	2.4	

DC Electrical Characteristics Continued (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Output High (Source) Current	I_{OH}	5V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 2.5V	-2.0	-1.6	-1.15	mA
		5V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 4.6V	-0.64	-0.42	-0.36	
		10V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 9.5V	-1.6	-1.1	-0.9	
		15V	V_{IN} = V_{DD} or V_{SS} V_{OH} = 13.5V	-4.2	-2.8	-2.4	
Maximum Positive-Going Input Threshold Voltage	$V_{T+ MAX}$	5V	Input A or B; other inputs V_{DD}	3.6	3.6	3.6	V
		10V		7.1	7.1	7.1	
		15V		10.8	10.8	10.8	
		5V	Input A and B; other inputs V_{DD}	4.0	4.0	4.0	V
		10V		8.2	8.2	8.2	
		15V		12.7	12.7	12.7	
Minimum Positive-Going Input Threshold Voltage	$V_{T+ MIN}$	5V	Input A or B; other inputs V_{DD}	2.2	2.2	2.2	V
		10V		4.6	4.6	4.6	
		15V		6.8	6.8	6.8	
		5V	Input A and B; other inputs V_{DD}	2.6	2.6	2.6	V
		10V		5.6	5.6	5.6	
		15V		6.3	6.3	6.3	
Maximum Negative-Going Input Threshold Voltage	$V_{T- MAX}$	5V	Input A or B; other inputs V_{DD}	2.8	2.8	2.8	V
		10V		5.2	5.2	5.2	
		15V		7.4	7.4	7.4	
		5V	Input A or B; other inputs V_{DD} Input A and B; other inputs V_{DD}	3.2	3.2	3.2	V
		10V		6.6	6.6	6.6	
		15V		9.6	9.6	9.6	
Minimum Negative-Going Input Threshold Voltage	$V_{T- MIN}$	5V	Input A or B; other inputs V_{DD}	0.9	0.9	0.9	V
		10V		2.5	2.5	2.5	
		15V		4	4	4	
		5V	Input A and B; other inputs V_{DD}	1.4	1.4	1.4	V
		10V		3.4	3.4	3.4	
		15V		4.8	4.8	4.8	

4. -55°C ≤ T_J ≤ +125°C

DC Electrical Characteristics Continued (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Hysteresis Voltage[3]	$V_{H\ MAX}$	5V	Input A or B; other inputs V_{DD}	1.6	1.6	1.6	V
		10V		3.4	3.4	3.4	
		15V		5	5	5	
		5V	Input A and B; other inputs V_{DD}	1.6	1.6	1.6	V
		10V		3.4	3.4	3.4	
		15V		5	5	5	
Minimum Hysteresis Voltage[5]	$V_{H\ MIN}$	5V	Input A or B; other inputs V_{DD}	0.3	0.3	0.3	V
		10V		1.2	1.2	1.2	
		15V		1.6	1.6	1.6	
		5V	Input A and B; other inputs V_{DD}	0.3	0.3	0.3	V
		10V		1.2	1.2	1.2	
		15V		1.6	1.6	1.6	

5. $V_{H\ MIN} > (V_{T+\ MIN}) - (V_{T-\ MAX})$; $V_{H\ MAX} = (V_{T+\ MAX}) + (V_{T-\ MIN})$

AC Electrical Characteristics[6]

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	TYPICAL	LIMITS		UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input to Output (Figure 1)	t_{PLH}, t_{PHL}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	380	380	760	ns
		10V		180	180	360	
		15V		130	130	260	
Maximum Output Transition Time, Any Output (Figure 1)	t_{TLH}, t_{THL}	5V	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	200	200	400	ns
		10V		100	100	200	
		15V		80	80	160	
Maximum Input Capacitance	C_{IN}	-	C_L = 50pF, R_L = 200kΩ $t_r = t_f$ = 20ns	5	7.5	7.5	pF

6. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

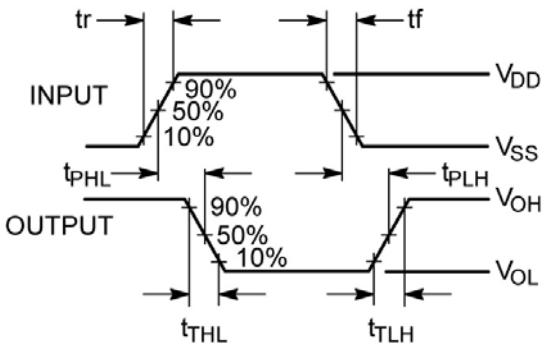


Figure 1 – Propagation Delay, Output Timing