



CMOS High Voltage Logic – CD4049B

Hex Inverter / Buffer Logic IC in bare die form

Rev 1.0
21/11/17

Description

The CD4049B Inverting Hex Buffer is fabricated on a 3µm 15CMOS process. The device is typically used as a Hex Buffer, CMOS to TTL converter or as a CMOS current driver. Logic levels are converted using only one supply voltage (V_{DD}). Special input protection allows the input signal high level (V_{IH}) to exceed the V_{DD} supply voltage when the device is used for logic level conversion. Two TTL/DTL loads can be driven over the full temperature range when the devices are used as level converters.

Features:

- High Input Voltage up to 20V
- Inputs allow voltages greater than V_D
- High Source and Sink Currents
- x2 TTL load drive over Military Temperature range
- Specified at 5V, 10V & 15V
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

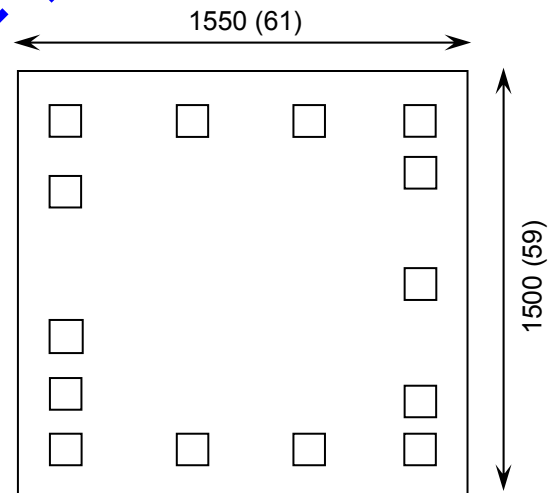
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com/quality/bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- ~~Sawn Wafer on Tape~~ – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1550 x 1500 61 x 59	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

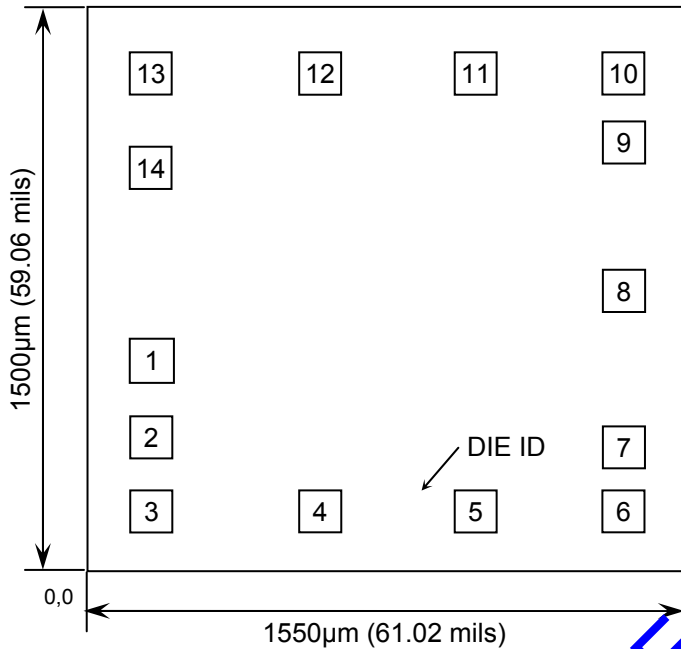




CMOS High Voltage Logic – CD4049B

Rev 1.0
21/11/17

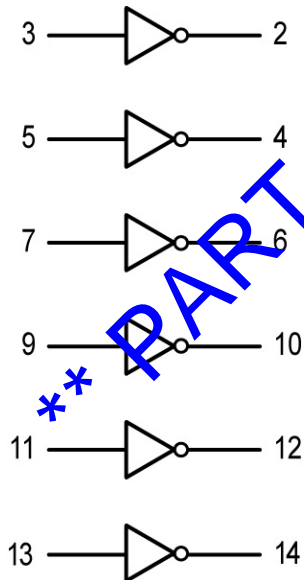
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	V _{DD}	0.110	0.505
2	1Y	0.110	0.305
3	1A	0.110	0.110
4	2Y	0.542	0.110
5	2A	0.982	0.110
6	3Y	1.320	0.110
7	3A	1.320	0.280
8	V _{SS}	1.320	0.700
9	4A	1.320	1.090
10	4Y	1.320	1.270
11	5A	0.942	1.270
12	5Y	0.542	1.270
13	6A	0.110	1.270
14	6Y	0.110	1.020

CONNECT CHIP BACK TO V_{DD} OR FLOAT

Logic Diagram



PAD 1 = V_{DD}
PAD 8 = V_{SS}

Truth Table

INPUTS		OUTPUT
A		Y
H		L
L		H

H = High level (steady state)
L = Low level (steady state)





CMOS High Voltage Logic – CD4049B

Rev 1.0

21/11/17

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to V_{SS})	V_{DD}	-0.5 to +20	V
DC Input Voltage ² (Referenced to V_{SS})	V_{IN}	V_{DD} to +18	V
DC Output Voltage (Referenced to V_{SS})	V_{OUT}	-0.5 to $V_{DD}+0.5$	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}, I_{OUT}	±10	mA
Power Dissipation in Still Air ²	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	3.0	18	V
DC Input Voltage ⁴	V_{IN}	0	V_{DD}	V
Operating Temperature Range	T_J	-55	+125	°C

3. This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referred to the V_{SS} pad only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, the ranges $V_{SS} \leq V_{IN} \leq 18$ V and $V_{SS} \leq V_{OUT} \leq V_{DD}$ are recommended. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. 4. $V_{IN} \leq V_{DD}$ is not recommended. High-to-Low level conversion only.

DC Electrical Characteristics (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum High-Level Input Voltage	V_{IH}	5V	$V_{OUT} = 0.5V$	4	4	4	V
		10V	$V_{OUT} = 1.0V$	8	8	8	
		15V	$V_{OUT} = 1.5V$	12.5	12.5	12.5	
Maximum Low-Level Input Voltage	V_{IL}	5V	$V_{OUT} = V_{DD} - 0.5V$	1	1	1	V
		10V	$V_{OUT} = V_{DD} - 1.0V$	2	2	2	
		15V	$V_{OUT} = V_{DD} - 1.5V$	2.5	2.5	2.5	
Minimum High-Level Output Voltage	V_{OH}	5V	$V_{IN} = V_{SS}$	4.95	4.95	4.95	V
		10V		9.95	9.95	9.95	
		15V		14.95	14.95	14.95	
Maximum Low-Level Output Voltage	V_{OL}	5V	$V_{IN} = V_{DD}$	0.05	0.05	0.05	V
		10V		0.05	0.05	0.05	
		15V		0.05	0.05	0.05	
Maximum Input Leakage Current	I_{IN}	18V	$V_{IN} = V_{DD}$ or V_{SS}	±0.1	±0.1	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{DD}	5V	$V_{IN} = V_{DD}$ or V_{SS} $I_{OUT} = 0\mu A$	1	1	30	µA
		10V		2	2	60	
		15V		4	4	120	
		20V		20	20	600	





CMOS High Voltage Logic – CD4049B

Rev 1.0

21/11/17

DC Electrical Characteristics Continued (Voltages referenced to V_{SS})

PARAMETER	SYMBOL	V_{DD}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum Output Low (Sink) Current	I_{OL}	4.5V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	3.3	2.6	1.8	mA
		5V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	4	3.2	2.4	
		10V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.5V$	10	8	5.6	
		15V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 1.5V$	26	21	18	
Minimum Output High (Source) Current	I_{OH}	5V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = 2.5V$	-2.6	-2.1	-1.55	mA
		5V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = 4.6V$	-0.81	-0.65	-0.48	
		10V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = 9.5V$	-2.0	-1.65	-1.18	
		15V	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = 13.5V$	-5.2	-4.3	-3.1	

5. $-55^{\circ}C \leq T_J \leq +125^{\circ}C$

AC Electrical Characteristics⁶

PARAMETER	SYMBOL	V_{IN}	V_{DD}	CONDITIONS	LIMITS			UNITS
					25°C	85°C	FULL RANGE ⁵	
Maximum Propagation Delay, Input A to Output Y (Figure 1)	t_{PLH}	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	120	120	240	ns
		10V	10V		65	65	130	
		10V	5V		90	90	180	
		15V	15V		50	50	100	
		15V	5V		90	90	180	
Maximum Propagation Delay, Input A to Output X (Figure 1)	t_{PHL}	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	65	65	130	ns
		10V	10V		40	40	80	
		10V	5V		30	30	60	
		15V	15V		30	30	60	
		15V	5V		20	20	40	
* Output Transition Time, Any Output (Figure 1)	t_{TLH}	5V	5V	$C_L = 50pF$, $R_L = 200k\Omega$ $t_r = t_f = 20ns$	160	160	320	ns
		10V	10V		80	80	160	
		15V	15V		60	60	120	

6. Not production tested in die form, characterized by chip design and tested in package.





CMOS High Voltage Logic – CD4049B

Rev 1.0
21/11/17

AC Electrical Characteristics Continued⁶

PARAMETER	SYMBOL	V _{IN}	V _{DD}	CONDITIONS	LIMITS			UNITS
					25°C	85°C	FULL RANGE ⁵	
Output Transition Time, Any Output (Figure 1)	t _{THL}	5V	5V	C _L = 50pF, R _L = 200kΩ t _r = t _f = 20ns	60	60	120	ns
		10V	10V		40	40	80	
		15V	15V		30	30	60	
Input Capacitance	C _{IN}	-		C _L = 50pF, R _L = 200kΩ t _r = t _f = 20ns	22.5	22.5	22.5	pF

6. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveform

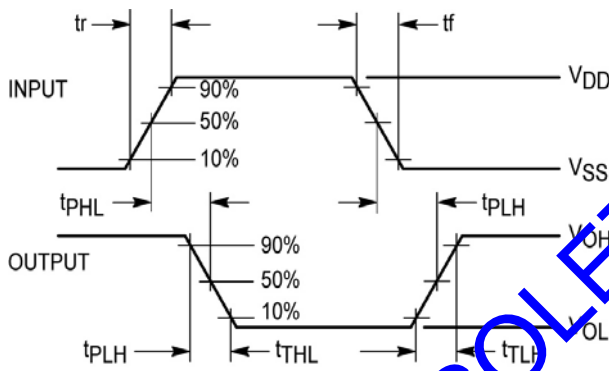


Figure 1 – Input to Output

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

