Monolithic Transistor Array – SiS3045

Silicon General Purpose x5 NPN Transistor array in bare die form

Rev 1.1
20/10/17

Description

The SiS3045 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits however; in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The SiS3045 is a direct electrical & mechanical replacement for the obsolete Intersil CA3045 & National (TI) LM3045.

Features:

- Two matched transistors:
  - V_{BE} Match ±5mA
  - I_{IO} Match 2μA (Max)
- Low Noise Figure 3.2dB (Typ) at 1kHz
- Operation From DC to 120MHz
- Wide Operating Current Range
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

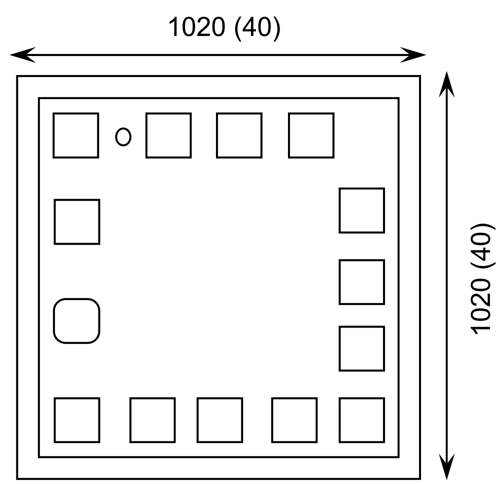
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in μm (mils)



Supply Formats:

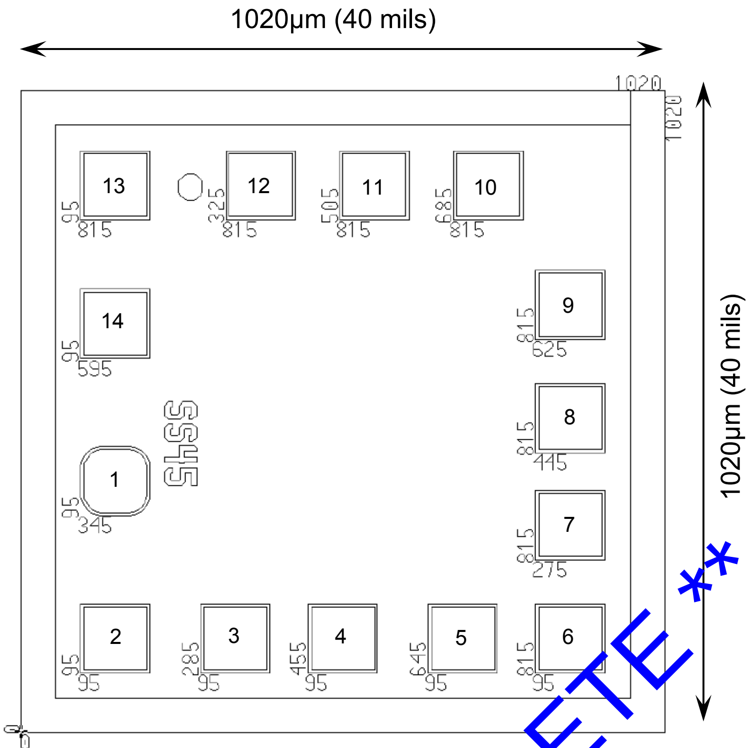
- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – By specific request
- Unsawn Wafer – By specific request
- 14 Lead CERDIP / PDIP package – By specific request
- 14 Lead SOIC package – By specific request

Mechanical Specification

Die Size (Unsawn)	1020 x 1020 40 x 40	μm mils
Minimum Bond Pad Size	100 x 100 4 x 4	μm mils
Die Thickness	460 18.1	μm mils
Top Metal Composition	TiW-AlSi 0.15μm-3μm	
Back Metal Composition	N/A – Bare Si	

Rev 1.1
20/10/17

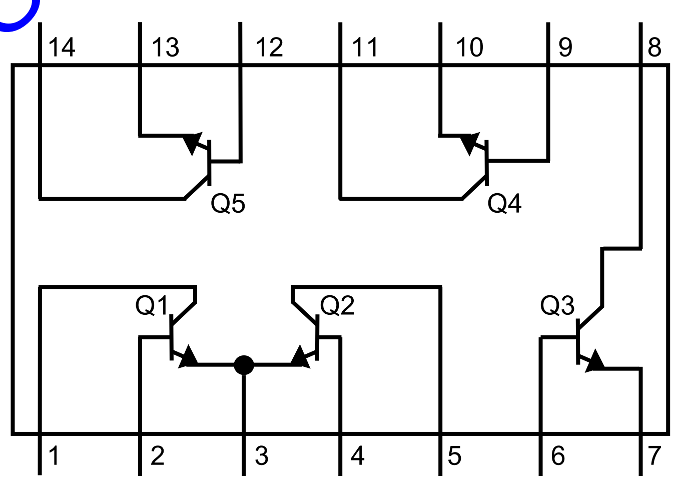
Pad Layout and Functions



PAD	FUNCTION
1	COLLECTOR Q1
2	BASE Q1
3	EMITTERS Q1 & Q2
4	BASE Q2
5	COLLECTOR Q2
6	BASE Q3
7	EMITTER Q3
8	COLLECTOR Q3
9	BASE Q4
10	EMITTER Q4
11	COLLECTOR Q4
12	BASE Q5
13	EMITTER Q5 & SUBSTRATE
14	COLLECTOR Q5

Die backside must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Circuit Schematic



Monolithic Transistor Array – SiS3045

Rev 1.1
20/10/17

Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Collector-to-Substrate Voltage (Note 1)	V_{CIO}	20	V
Emitter-to-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Maximum Power Dissipation (Any one transistor)	P_D	300	mW
Operating Temperature Range	-	-55 to 125	°C
Maximum Junction Temperature	T_J	175	°C

DC Electrical Characteristics T_A = 25°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E= 0		20	60	-	V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C= 0		5	7	-	V
Collector Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	40	nA
Collector Cutoff Current (Figure 2)	I_{CEO}	V_{CE} = 10V, I_B = 0		-	FIG 2	0.5	µA
Forward Current Transfer Ratio (Static Beta) (Note 3) (Figure 3)	h_{FE}	V_{CE} =3V	I_C = 10mA	-	100	-	-
			I_C = 1mA	40	100	-	-
			I_C = 10µA	-	54	-	-
Input Offset Current for Matched Pair Q1 and Q2. (Note 2) (Figure 4)	$\lvert I_{IO1} - I_{IO2}\rvert$	V_{CE} = 3V, I_C = 1mA		-	0.3	2	µA
Base-to-Emitter Voltage (Note 2) (Figure 5)	V_{BE}	V_{CE} = 3V	I_E = 1mA	-	0.715	-	V
			I_E =10mA	-	0.800	-	
Magnitude of Input Offset Voltage for Differential Pair (Note 2) (Figures 5, 7)	$\lvert V_{BE1} - V_{BE2}\rvert$	V_{CE} = 3V, I_C = 1mA		-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors. (Note 2) (Figures 5, 7)	$\lvert V_{BE3} - V_{BE4}\rvert$ $\lvert V_{BE4} - V_{BE5}\rvert$ $\lvert V_{BE5} - V_{BE3}\rvert$	V_{CE} = 3V, I_C = 1mA		-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3V, I_C = 1mA		-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1mA, I_C = 10mA		-	0.23	-	V
Temperature Coefficient: Magnitude of Input Offset Voltage (Figure 7)	$\frac{\lvert \Delta V_{IO}\rvert}{\Delta T}$	V_{CE} = 3V, I_C = 1mA		-	1.1	-	µV/°C

Notes: **1.** The collector of each transistor is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. **2.** Actual forcing current is via the emitter for this test.

Rev 1.1
20/10/17

Dynamic Electrical Characteristics T_A = 25°C unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Noise Figure (Figure 9)	NF	f = 1 kHz, V_{CE} = 3V I_C = 100μA, Source Resistance = 1kΩ	-	3.25	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics						
Forward Current Transfer Ratio (Figure 11)	h_{FE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	110	-	-
Short Circuit Input Impedance (Figure 11)	h_{IE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 11)	h_{OE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	15.6	-	μmho
Open Circuit Reverse Voltage Transfer Ratio (Figure 11)	h_{RE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	1.8 x 10^{-4}	-	-
Admittance Characteristics						
Forward Transfer Admittance (Figure 12)	Y_{FE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	31 - j1.5	-	-
Input Admittance (Figure 13)	Y_{IE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	0.3 + j0.04	-	-
Output Admittance (Figure 14)	Y_{OE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	0.001+j0.03	-	-
Reverse Transfer Admittance (Figure 15)	Y_{RE}	f = 1 kHz V_{CE} = 3V, I_C = 1mA	-	Fig 14	-	-
Gain Bandwidth Product (Figure 16)	f_T	V_{CE} = 3V, I_C = 1mA	300	550	-	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3V, I_C = 0	-	2.8	-	pF

Typical Performance Characteristics

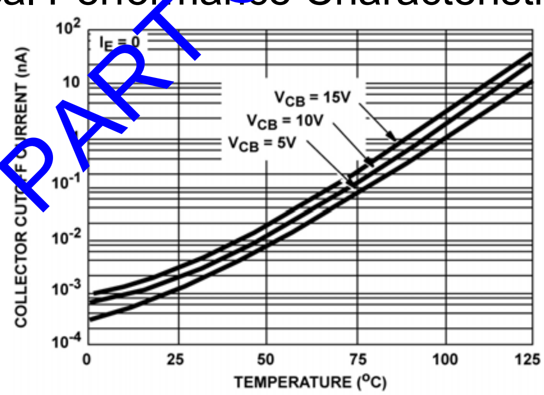


FIGURE 1. Typical Base-To-Collector Current vs Temperature (each transistor)

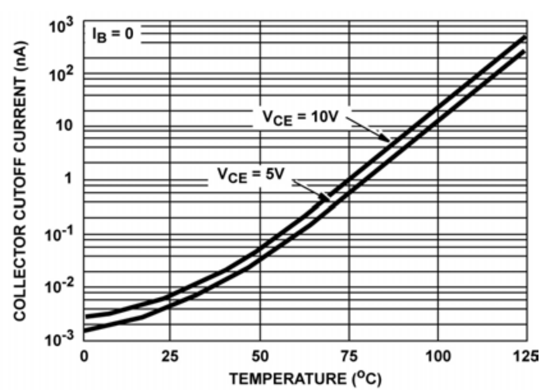


FIGURE 2. Typical Collector-To-Emitter Cutoff Current vs Temperature (each transistor)

Typical Performance Characteristics (Continued)

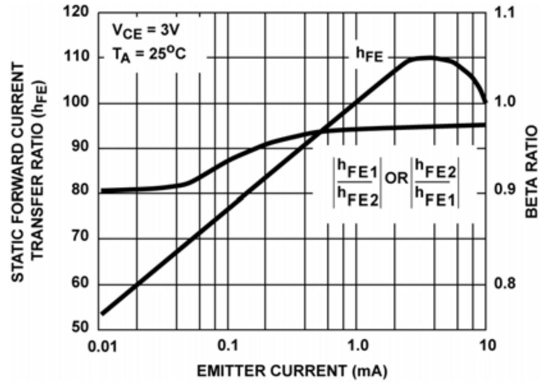


FIGURE 3. Typical Static Forward Current Transfer Ratio & Beta Ratio for Q_1 and Q_2 vs Emitter Current

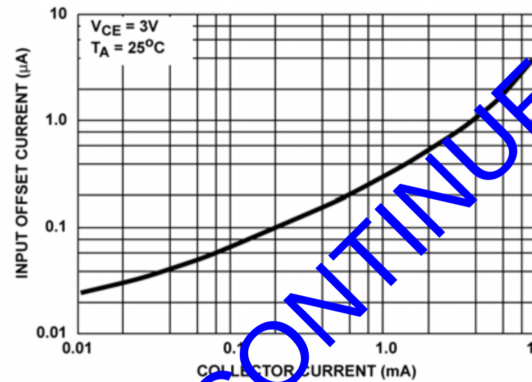


FIGURE 4. Typical Input Offset Current for matched transistor pair Q_1Q_2 vs Collector Current

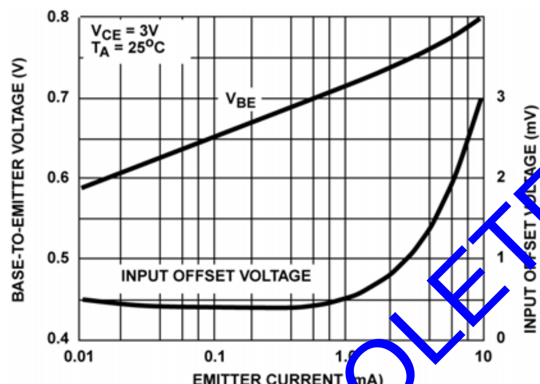


FIGURE 5. Typical static Base-to-Emitter Voltage characteristics and Input Offset Voltage for differential pair and paired isolated transistors vs Emitter Current

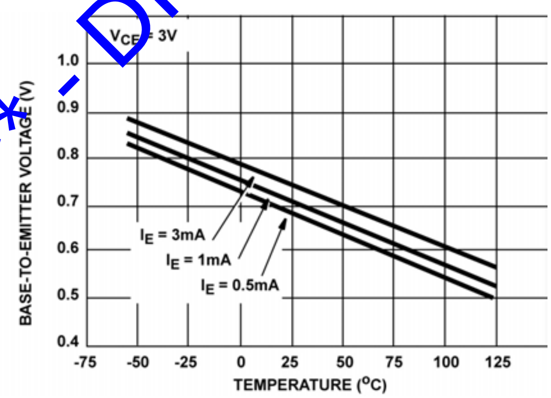


FIGURE 6. Typical Base-to-Emitter Voltage characteristic vs Temperature for each transistor.

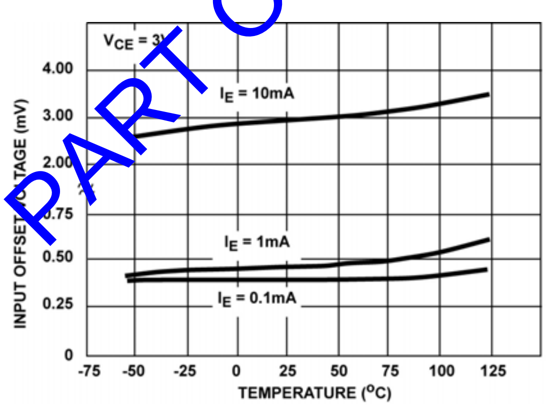


FIGURE 7. Typical Input Offset Voltage characteristics for differential pair and paired isolated transistors vs Temperature

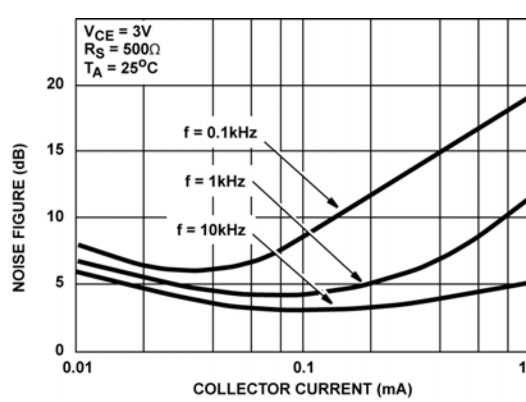


FIGURE 8. Typical Noise Figure vs Collector Current

Typical Performance Characteristics (Continued)

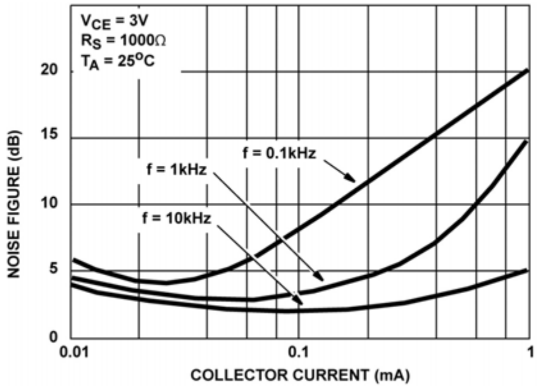


FIGURE 9. Typical Noise Figure vs Collector Current

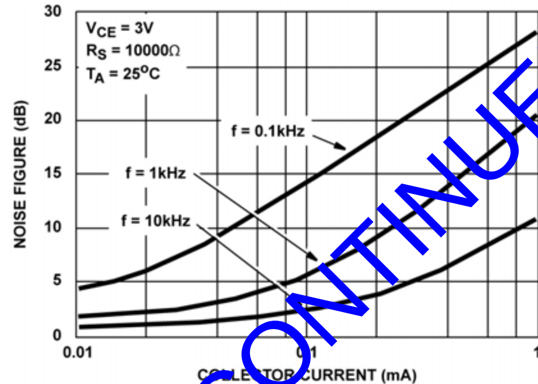


FIGURE 10. Typical Noise Figure vs Collector Current

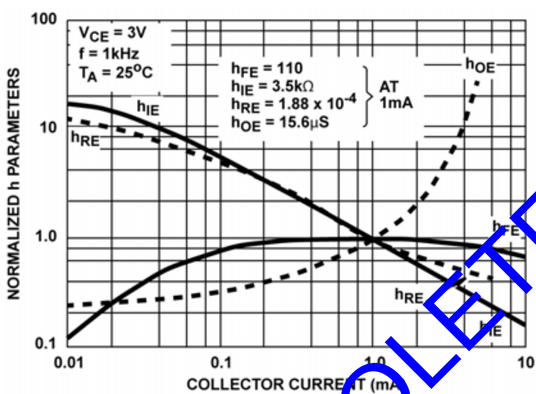


FIGURE 11. Typical Normalized Forward Current Transfer ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, And Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

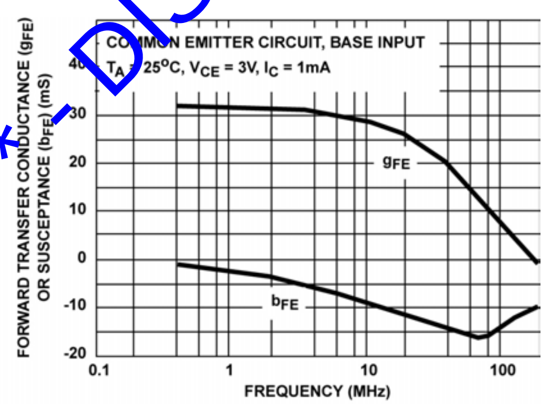


FIGURE 12. Typical Forward Transfer Admittance vs Frequency

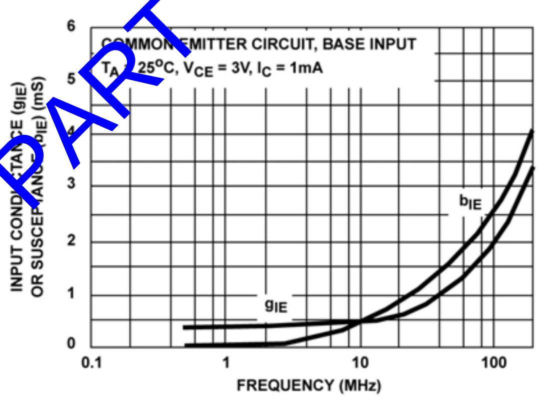


FIGURE 13. Typical Input Admittance vs Frequency

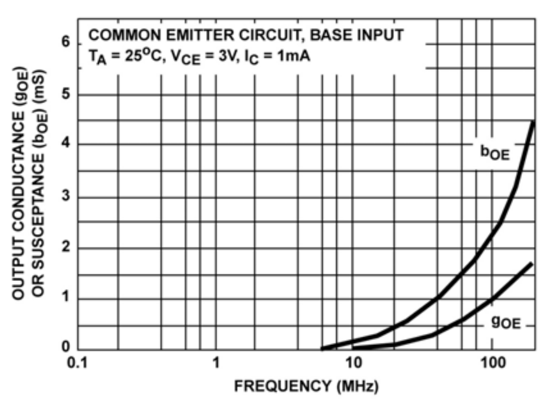


FIGURE 14. Typical Output Admittance vs Frequency

Typical Performance Characteristics (Continued)

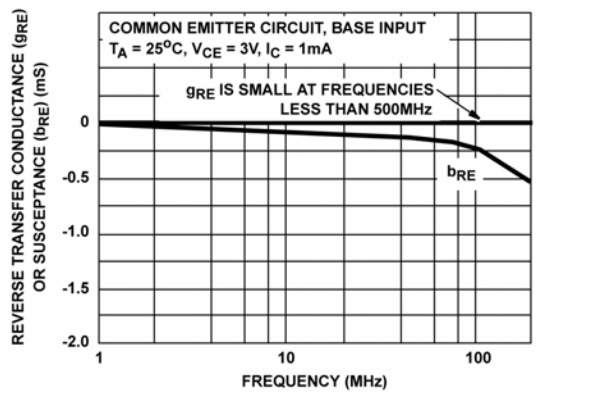


FIGURE 15. Typical Reverse Transfer Admittance vs Frequency

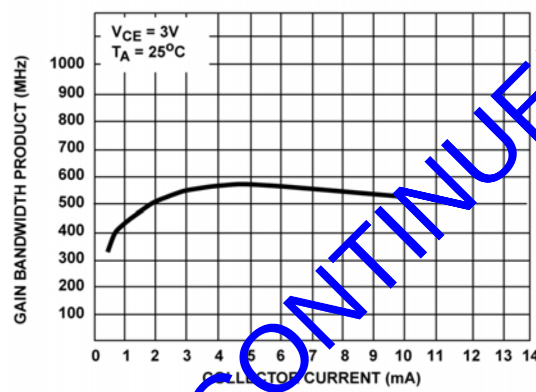


FIGURE 16. Typical Gain Bandwidth Product vs Collector Current

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.