



# Low Power Schottky Logic – 74LS04

## Hex Inverter Gates Logic IC in bare die form

Rev 1.0  
24/11/17

### Description

The 74LS04 Hex Inverter is fabricated using a 2µm 40V Bipolar process. The device contains six independent inverters with standard push-pull outputs which perform the Boolean function  $Y = \bar{A}$  in positive logic.

### Features:

- High speed – 19ns (Typ) propagation delay
- Direct drop-in replacement for obsolete components in long term programs.

### Ordering Information

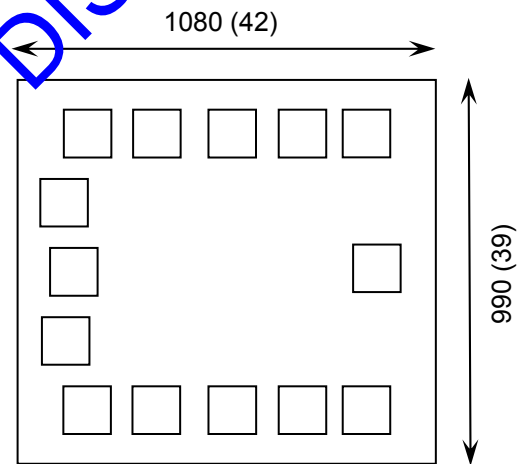
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54LS04](#)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- ~~Sawn Wafer on Tape~~ – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1080 x 990 42 x 39	µm mils
Minimum Bond Pad Size	116 x 116 4.6 x 4.6	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

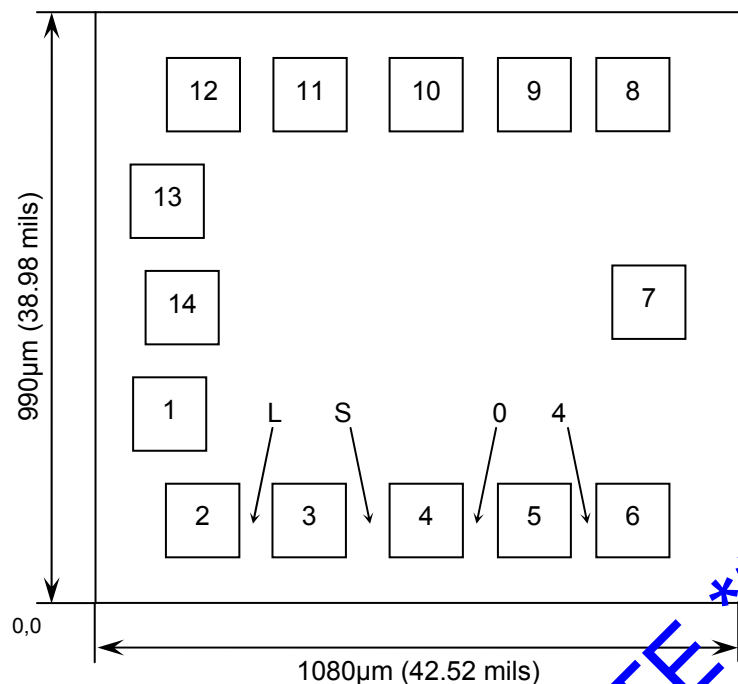




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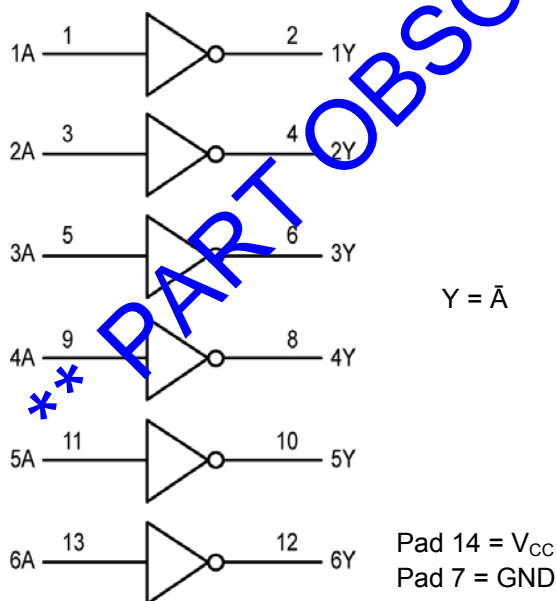
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.073	0.268
2	1Y	0.132	0.092
3	2A	0.308	0.092
4	2Y	0.503	0.092
5	3A	0.685	0.092
6	3Y	0.854	0.092
7	GND	0.880	0.456
8	4Y	0.854	0.804
9	4A	0.685	0.804
10	Y5	0.503	0.804
11	5A	0.308	0.804
12	6Y	0.132	0.804
13	6A	0.073	0.628
14	V <sub>CC</sub>	0.094	0.450

CONNECT CHIP BACK TO GND OR FLOAT

## Logic Diagram



## Truth Table

INPUTS		OUTPUT
A		Y
H		L
L		H

H = High level (steady state)  
L = Low level (steady state)





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	$V_{CC}$	7.0	V
DC Input Voltage	$V_{IN}$	7.0	V
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

## Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{CC}$	4.75	5.25	V
High-Level Input Voltage	$V_{IH}$	2	-	V
Low-Level Input Voltage	$V_{IL}$	-	0.8	V
High-Level Output Current	$I_{OH}$	-	-0.4	mA
Low-Level Output Current	$I_{OL}$	-	8	mA
Operating Temperature Range	$T_J$	0	+85	°C

## DC Electrical Characteristics<sup>2</sup> $T_J = 0^\circ\text{C}$ to $85^\circ\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum High-Level Input Voltage	$V_{IH}$	-	2	-	-	V
Maximum Low-Level Input Voltage	$V_{IL}$	-	-	-	0.8	V
Input Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{MIN}$ $I_{IN} = -18\text{mA}$	-	-0.65	-1.5	V
Output Voltage High	$V_{OH}$	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$ $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table	2.7	3.5	-	V
Output Voltage Low	$V_{OL}$	$V_{CC} = V_{CC} \text{ MIN}$ $I_{OH} = \text{MAX}$ $V_{IN} = V_{IL}$ or $V_{IH}$ per Truth Table $I_{OL} = 8\text{mA}$	-	0.35	0.5	V
Input High Current	$I_{IH}$	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	-	-	20	$\mu\text{A}$
		$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$	-	-	0.1	mA
Input Low Current	$I_{IL}$	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	-	-	-0.4	mA
Short Circuit Current <sup>3</sup>	$I_{OS}$	$V_{CC} = \text{MAX}$	-20	-	-100	mA
Power Supply Current (Total)	$I_{CC}$	$V_{CC} = \text{MAX}$ , Output High	-	1.2	2.4	mA
		$V_{CC} = \text{MAX}$ , Output Low	-	3.6	6.6	

2. All typical values @  $V_{CC} = 5\text{V}$ ,  $T_J = 25^\circ\text{C}$ . 3. Not more than one output should be shorted at a time, nor for more than 1 second.





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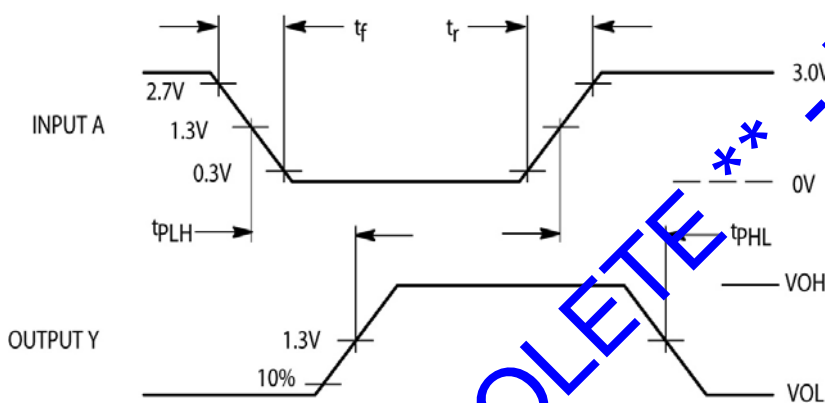
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## AC Electrical Characteristics<sup>4</sup>

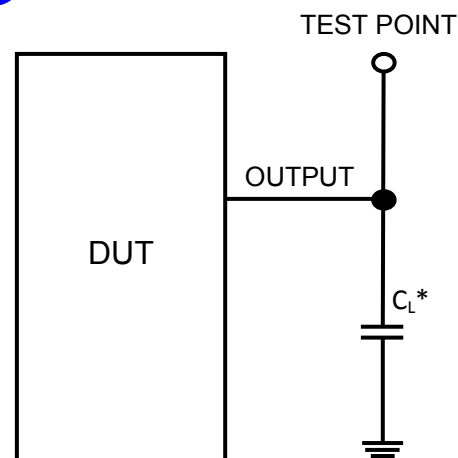
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Turn-Off Delay, Input to Output	$t_{PLH}$	$V_{CC} = 5V, C_L = 15pF$	-	9.0	15	ns
Turn-On Delay, Input to Output	$t_{PHL}$	$V_{CC} = 5V, C_L = 15pF$	-	10	15	

4. Not production tested in die form, characterized by chip design and tested in package.

## Switching Waveform



## Test Circuit



\* Includes all probe and jig capacitance

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