



# High Speed CMOS TTL Input – 74HCT00

Quad 2-Input NAND Gates with LSTTL compatible inputs in bare die form

Rev 1.0  
07/02/19

## Description

74HCT00 provides x4 independent 2-input NAND gates performing the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$ . The device is fabricated using a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. Internal circuitry comprises of 3 stages and includes buffered outputs for high noise immunity and stability. Device inputs directly accept both standard CMOS and LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

## Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- TTL / CMOS compatible Input Levels
- Function compatible with 74LS00.

## Ordering Information

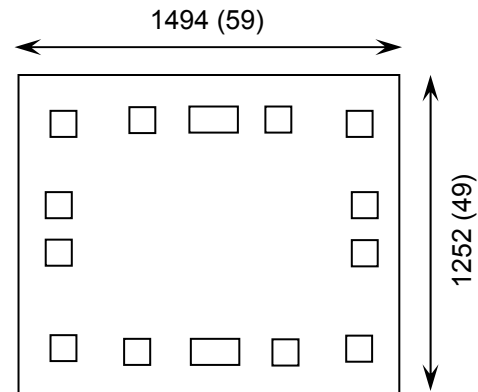
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54HCT00](#)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- ~~Sawn Wafer on Tape~~ – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1494 x 1252 59 x 59	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

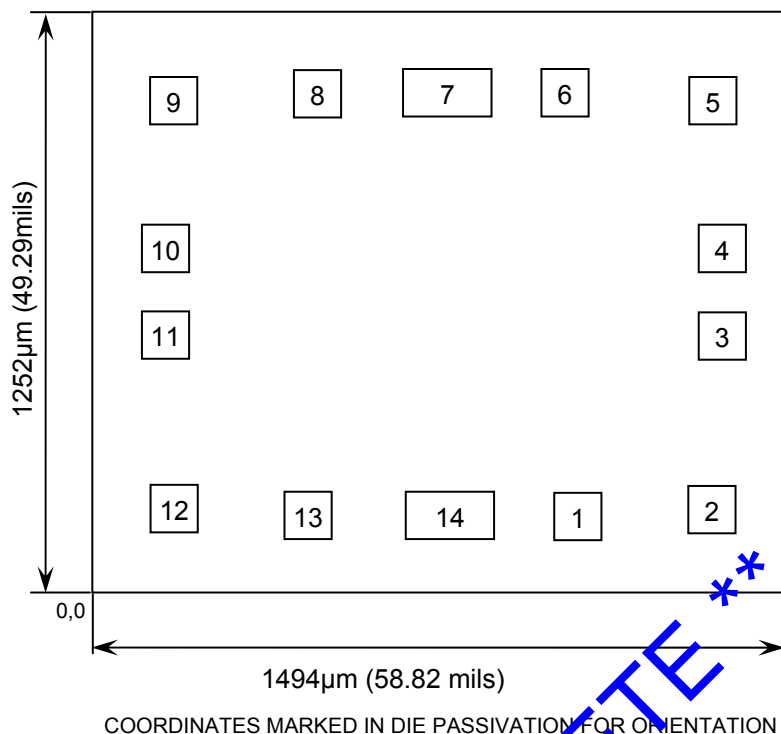




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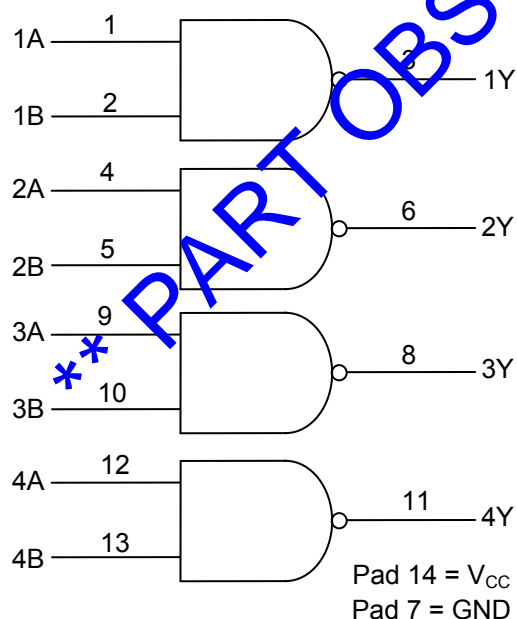
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.127	0.439
2	1B	0.137	0.129
3	1Y	0.522	0.119
4	2A	0.712	0.119
5	2B	1.055	0.129
6	2Y	1.065	0.466
7	GND	1.065	0.685
8	3Y	1.065	1.028
9	3A	1.055	1.365
10	3B	0.712	1.375
11	4Y	0.522	1.375
12	4A	0.137	1.365
13	4B	0.127	1.055
14	V <sub>CC</sub>	0.127	0.679

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram



## Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High level (steady state)  
L = Low level (steady state)





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	$I_{IN}$	$\pm 20$	mA
DC Output Current, per pad	$I_{OUT}$	$\pm 25$	mA
DC Supply Current, $V_{CC}$ or GND, per pad	$I_{CC}$	$\pm 50$	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to +150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{CC}$	4.5	5.5	V
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V
Operating Temperature Range	$T_J$	0	+85	°C
Input Rise or Fall Times	$t_r, t_f$	-	500	ns

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	$V_{IH}$	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	2.0	2.0	2.0	V
		5.5V		2.0	2.0	2.0	
Maximum Low-Level Input Voltage	$V_{IL}$	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	$V_{OH}$	4.5V	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\mu A$	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0mA$	3.98	3.84	3.84	
Maximum Low-Level Output Voltage	$V_{OL}$	4.5V	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\mu A$	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0mA$	0.26	0.33	0.33	





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## DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current <sup>5</sup>	I <sub>CC</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND  I <sub>OUT</sub>   ≤ 0μA	1	10	10	μA
Additional Quiescent Supply Current <sup>5</sup>	ΔI <sub>CC</sub>	5.5V	V <sub>IN</sub> = 2.4V, Any One Input. V <sub>IN</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>OUT</sub> = 0μA	≥ 0°C	25°C to 85°C		mA
				2.9	2.4		

4. 0°C ≤ T<sub>J</sub> ≤ +85°C 5. Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

## AC Electrical Characteristics<sup>6</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Input A to Input Y (Figure 1,2)	t <sub>PLH</sub> , t <sub>PHL</sub>	5V ±10%	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	19	24	24	ns
Maximum Output Rise and Fall Time (Figure 1,2)	t <sub>TLH</sub> , t <sub>THL</sub>	5V ±10%	C <sub>L</sub> = 50pF, t <sub>r</sub> = t <sub>f</sub> = 6ns	15	19	19	ns
Maximum Input Capacitance	C <sub>IN</sub>	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate <sup>7</sup>	C <sub>PD</sub>	-	T <sub>J</sub> = 25°C, V <sub>CC</sub> = 5.0V	TYPICAL			pF
				15			

6. Not production tested in die form, characterized by chip design and tested in package.

7. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

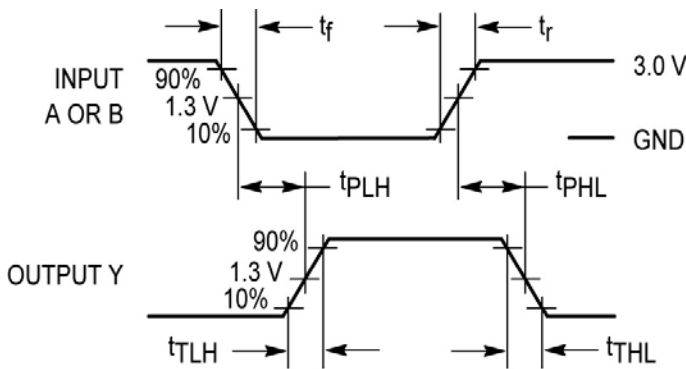




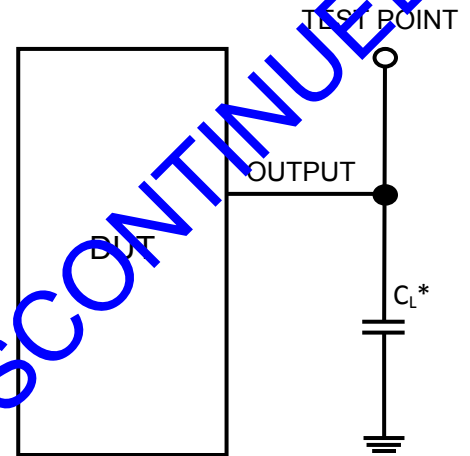
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## Switching Waveform



## Test Circuit



\* Includes all probe and jig capacitance

Figure 1 – Propagation Delay & Output Transition Time

Figure 2

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