High Speed CMOS Logic – 74HC393

Dual 4-bit negative edge triggered binary ripple counter in bare die form

Rev 1.0
7/5/2019

Description

The 74HC393 consists of x2 independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷ 256 counter can be produced by cascading the two binary counters. Internal flip–flops trigger by high–to–low transitions of the clock input. Reset for the counters is asynchronous & active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes & should not be used as clocks or as strobes except when gated with the Clock of the HC393.

Features:

- Low Input Current: 1µA
- Output Drive Capability: 10 LSTTL loads
- Outputs Directly Interface to CMOS, NMOS, & TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS393

Ordering Information

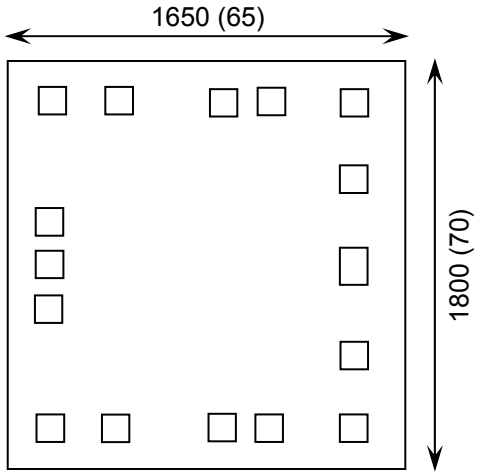
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC393

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1650 x 1800 65 x 70	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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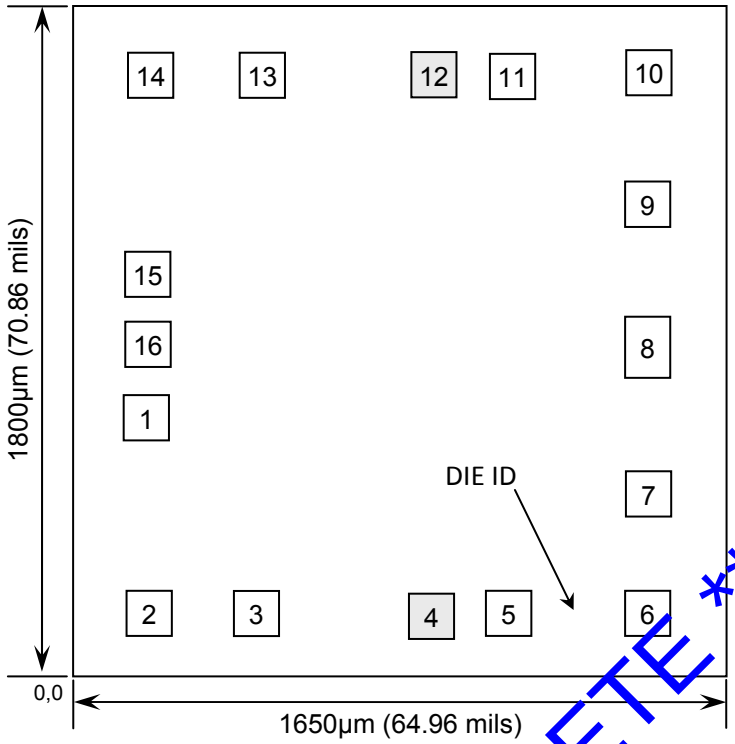
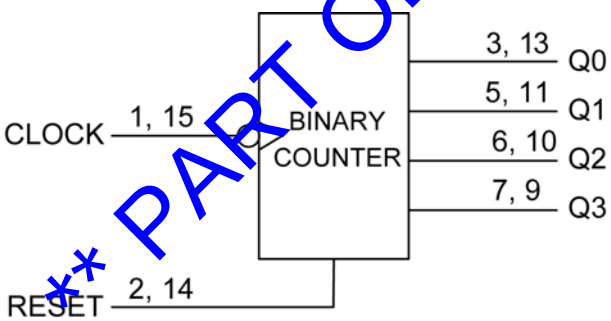
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1CP}$	0.112	0.657
2	1MR	0.122	0.122
3	1Q0	0.395	0.122
4	NC	0.842	0.122
5	1Q1	1.037	0.122
6	1Q2	1.386	0.122
7	1Q3	1.386	0.457
8	GND	1.386	0.817
9	2Q3	1.386	1.236
10	2Q2	1.386	1.572
11	2Q1	1.037	1.572
12	NC	0.842	1.572
13	2Q0	0.395	1.572
14	2MR	0.122	1.572
15	2CP	0.112	1.037
16	V_{CC}	0.112	0.847
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 16 = V_{CC}
Pad 8 = GND

Function Table

INPUTS		OUTPUTS
CLOCK	RESET	
X	H	L
H	L	NO CHANGE
L	L	NO CHANGE
↗	L	NO CHANGE
↘	L	ADVANCE TO NEXT STATE

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
DC Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-40	+85	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2.0V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	2V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	3.98	3.84	3.84	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	5.48	5.34	5.34	
Maximum Low-Level Output Voltage	V_{OL}	2V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.33	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.33	V
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	8	80	80	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency (50% Duty Cycle) (Figure 1, 3)	f_{MAX}	2V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	5.4	4.4	4.4	MHz
		4.5V		27	22	22	
		6.0V		32	26	26	
Maximum Propagation Delay, Clock to Q0 (Figure 1, 3)	t_{PLH}, t_{PHL}	2V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	120	150	150	ns
		4.5V		24	30	30	
		6.0V		20	26	26	
Maximum Propagation Delay, Clock to Q1 (Figure 1, 3)	t_{PLH}, t_{PHL}	2V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	190	240	240	ns
		4.5V		38	48	48	
		6.0V		32	41	41	
Maximum Propagation Delay, Clock to Q2 (Figure 1, 3)	t_{PLH}, t_{PHL}	2V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	240	300	300	ns
		4.5V		48	60	60	
		6.0V		41	51	51	

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AC Electrical Characteristics Continued[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Clock to Q3 (Figure 1, 3)	t_{PLH}, t_{PHL}	2V	C_L = 50pF, Input $t_r = t_f$ = 6ns	290	365	365	ns
		4.5V		58	73	73	
		6.0V		49	62	62	
Maximum Propagation Delay, Reset to any Q (Figure 2, 3)	t_{PHL}	2V	C_L = 50pF, Input $t_r = t_f$ = 6ns	165	205	205	ns
		4.5V		33	41	41	
		6.0V		28	35	35	
Maximum Output Transition Time, Any Output (Figure 1, 3)	t_{TLH}, t_{THL}	2V	C_L = 50pF, Input $t_r = t_f$ = 6ns	75	95	95	ns
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate[6]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				40			

5. Not production tested in die form, characterized by chip design and tested in package.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[5]	
Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	t_{rec}	2.0V	Input $t_r = t_f$ = 6ns	50	65	65	ns
		4.5V		10	13	13	
		6.0V		9	11	11	
Minimum Pulse Width, Clock (Figure 1)	t_w	2.0V	Input $t_r = t_f$ = 6ns	80	100	100	ns
		4.5V		16	20	20	
		6.0V		14	17	17	
Minimum Pulse Width, Reset (Figure 2)	t_w	2.0V	Input $t_r = t_f$ = 6ns	125	155	155	ns
		4.5V		25	31	31	
		6.0V		21	26	26	
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0V	Input $t_r = t_f$ = 6ns	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	

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Switching Waveform

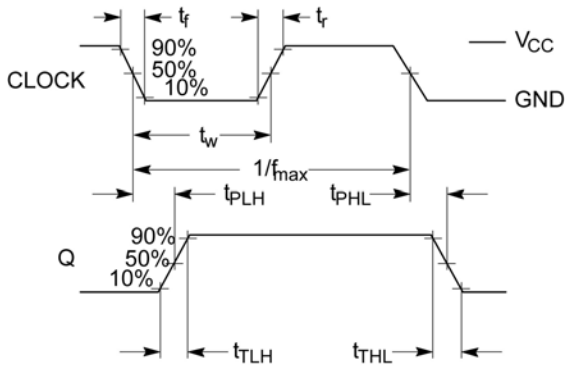


Figure 1 – Input to Output Propagation Delay & Timing

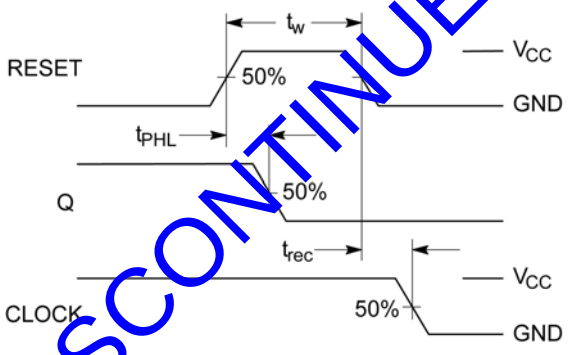
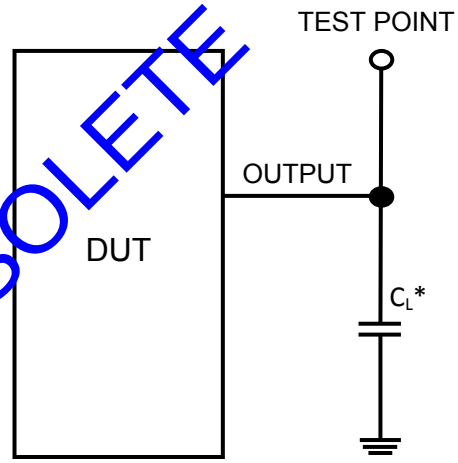


Figure 2 – Reset Timing

Test Circuit



* Includes all probe and jig capacitance

Figure 3