High Speed CMOS Logic – 74HC373

8-bit transparent D-Type Latch with 3-State Outputs in bare die form

Rev 1.0
10/03/21

Description

The 74HC373 consists of eight D-type transparent latches fabricated using a 2.5µm 5V CMOS process to combine high speed performance LSTTL performance with CMOS low power consumption. Each latch is equipped with separate D-Type inputs and 3-State outputs for bus oriented applications. Data output changes asynchronously and data may be latched even when the outputs are not enabled. Device inputs accept standard CMOS outputs or LSTTL outputs using pull-up resistors. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS373.

Ordering Information

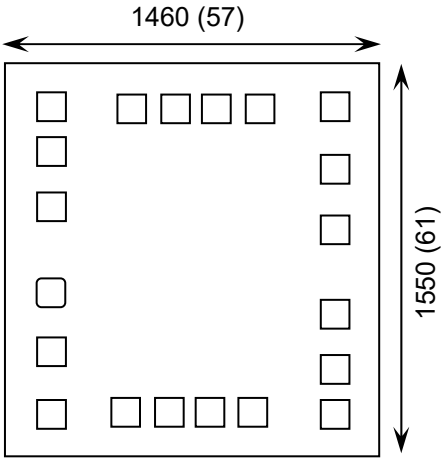
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC373

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1460 x 1550 57 x 61	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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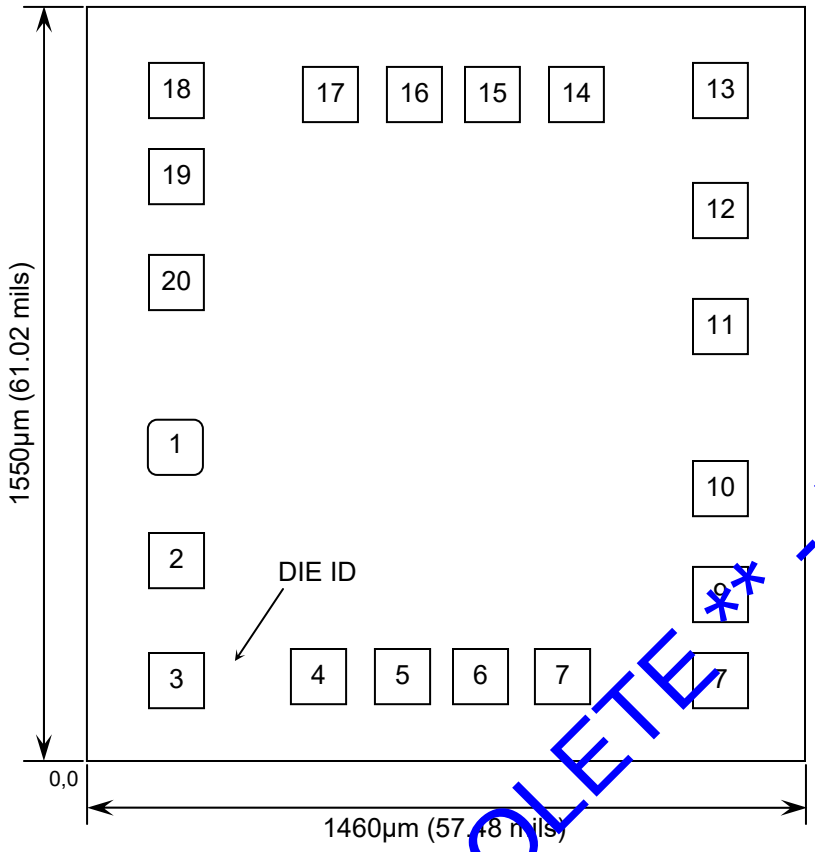
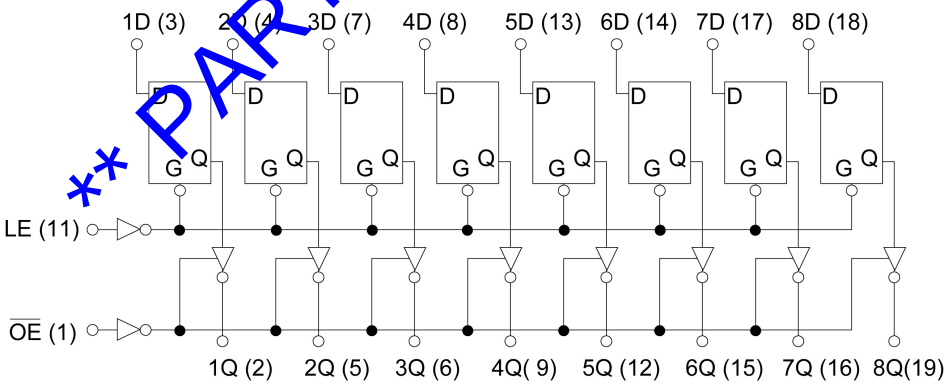
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{OE}$	0.1205	0.597
2	1Q	0.1205	0.3595
3	1D	0.1205	0.122
4	2D	0.413	0.1225
5	2Q	0.582	0.1225
6	3Q	0.7415	0.1225
7	3D	0.913	0.1225
8	4D	1.234	0.116
9	4Q	1.232	0.29
10	GND	1.232	0.51
11	LE	1.232	0.842
12	5Q	1.232	1.0795
13	5D	1.232	1.317
14	6D	0.9395	1.3165
15	6Q	0.7705	1.3165
16	7Q	0.611	1.3165
17	7D	0.4395	1.3165
18	8D	0.1185	1.323
19	8Q	0.1205	1.149
20	V_{CC}	0.1205	0.929
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 10 = GND, Pad 20 = V_{CC}

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±35	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±75	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-40	+85	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6.0V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\|I_{OUT}\|$ ≤ 20μA	0.5	0.5	0.5	V
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	
Minimum High-Level Output Voltage	V_{OH}	2V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 20μA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 6.0mA	3.98	3.84	3.84	V
		6.0V	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ ≤ 7.8mA	5.48	5.34	5.34	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 6.0mA$	0.26	0.33	0.33	V
		6.0V	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 7.8mA$	0.26	0.33	0.33	V
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$	4	40	40	µA
Maximum Three-State Leakage Current	I_{OZ}	6.0V	Output in High-Impedance State, $V_{IN} = V_{IH}$ or V_{IL}, $V_{OUT} = V_{CC}$ or GND	±0.5	±5.0	±5.0	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, D to Q, (Figure 1,5)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	125	155	155	ns
		4.5V		25	31	31	
		6.0V		21	26	26	
Maximum Propagation Delay, LE to Q, (Figure 2,5)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	140	175	175	ns
		4.5V		28	35	35	
		6.0V		24	30	30	
Maximum Propagation Delay, OE to Q (Figure 3,6)	t_{PLZ}, t_{PHZ}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	150	190	190	ns
		4.5V		30	38	38	
		6.0V		26	33	33	
Maximum Propagation Delay, OE to Q (Figure 3,6)	t_{PZL}, t_{PZH}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	150	190	190	ns
		4.5V		30	38	38	
		6.0V		26	33	33	

5 Not production tested in die form, characterized by chip design

AC Electrical Characteristics continued[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Output Transition Time, Any Output (Figure 1,5)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, Input t_r = t_f = 6ns	60	75	75	pF
		4.5V		12	15	15	
		6.0V		10	13	13	
Maximum Input Capacitance	C_{IN}	-	C_L = 50pF, Input t_r = t_f = 6ns	10	10	10	pF
Maximum 3-State Output Capacitance	C_{OUT}	-	C_L = 50pF, Input t_r = t_f = 6ns High Z state	15	15	15	pF
Power Dissipation Capacitance (Per latch)[7]	C_{PD}	5V	-	TYPICAL			pF
				36			

7. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to LE (Figure 4)	t_{SU}	2.0V	C_L = 50pF, Input t_r = t_f = 6ns	25	30	30	ns
		4.5V		5.0	6.0	6.0	
		6.0V		5.0	6.0	6.0	
Minimum Hold Time, LE to D (Figure 4)	t_h	2.0V	C_L = 50pF, Input t_r = t_f = 6ns	5.0	5.0	5.0	ns
		4.5V		5.0	5.0	5.0	
		6.0V		5.0	5.0	5.0	
Minimum Pulse Width, LE (Figure 4)	t_w	2.0V	C_L = 50pF, Input t_r = t_f = 6ns	60	75	75	ns
		4.5V		12	15	15	
		6.0V		10	13	13	
Maximum Input Rise & Fall Times (Figure 4)	t_r, t_f	2.0V	C_L = 50pF, Input t_r = t_f = 6ns	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	

Switching Waveforms

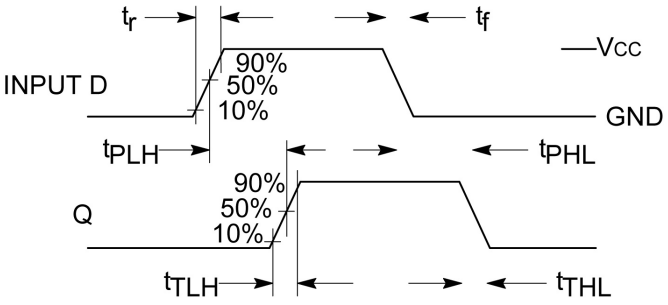


Figure 1 – Propagation Delay & Output Transition Time

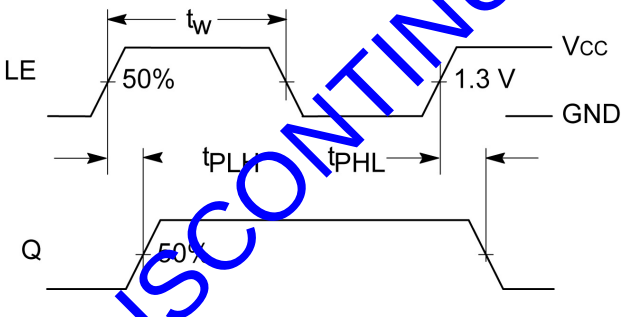


Figure 2 – Propagation Delay – Latch Enable to Q

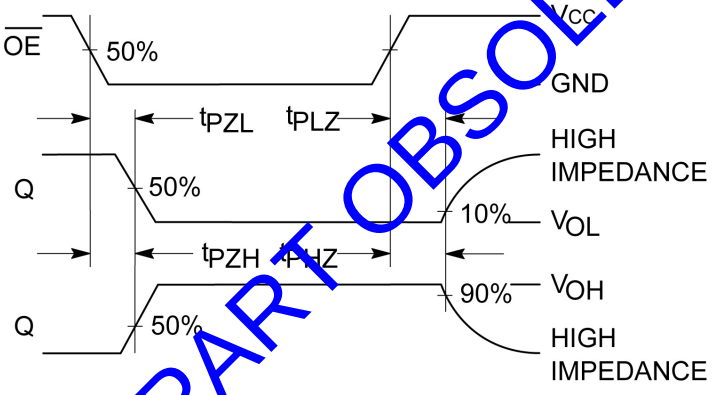


Figure 3 – Propagation Delay - Output Enable to Q

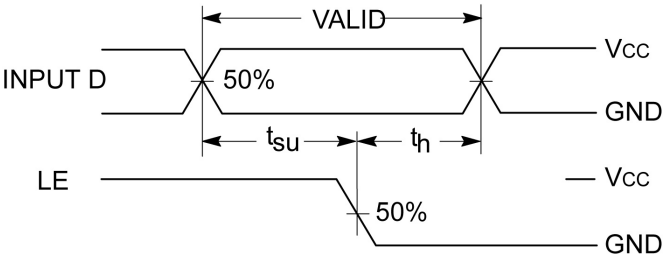
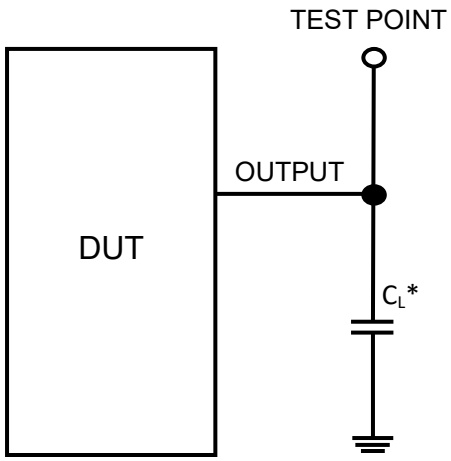


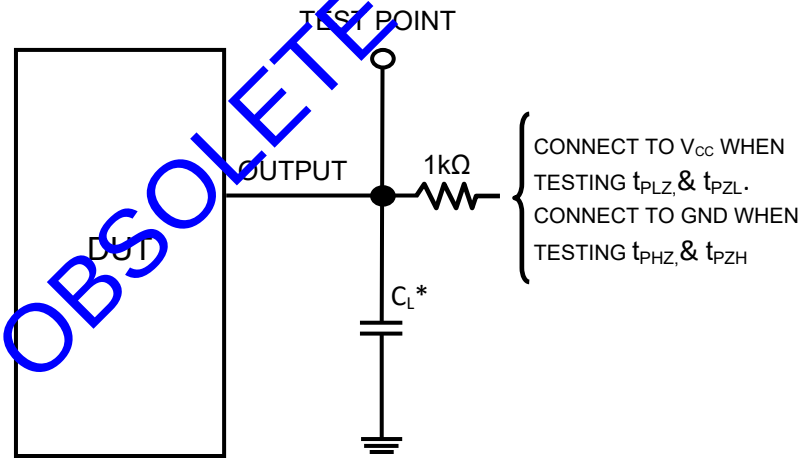
Figure 4 – Timing Requirements

Test Circuits



* Includes all probe and jig capacitance

Figure 5



* Includes all probe and jig capacitance

Figure 6