High Speed CMOS Logic – 74HC175

Quad D-Type Flip-Flop Logic IC with Reset in bare die form

Rev 1.0
21/11/17

Description

The 74HC175 is fabricated using a 2.5µm 5V CMOS process and consists of four D-Type flip–flops each with separate D input and common Reset and Clock inputs. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Reset is clock independent and is accomplished by a low level on the Reset line. The device is useful for applications where both the true and complement outputs are required and the clock and master reset are common to all storage elements.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Low Input Current: 1µA
- High Noise Immunity Characteristics of CMOS
- Operating Voltage Range: 2.0 to 6.0 V
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

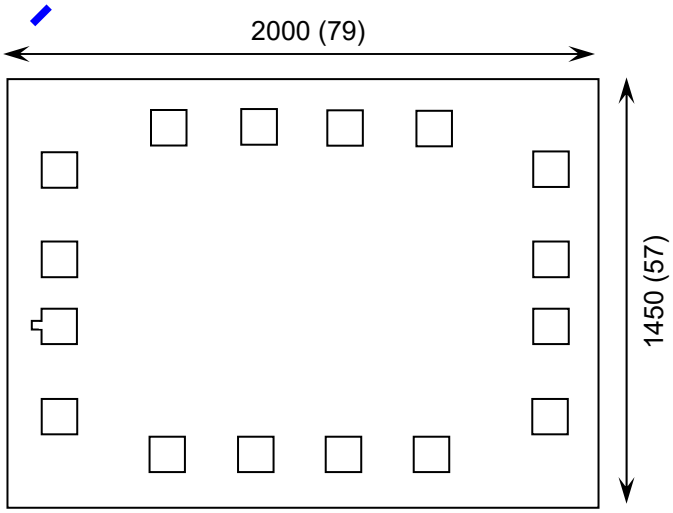
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC175

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	2000 x 1450 79 x 57	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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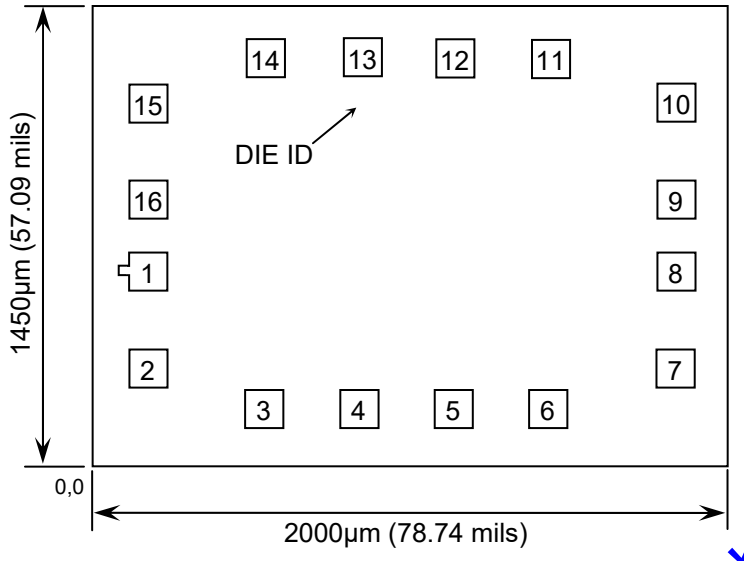
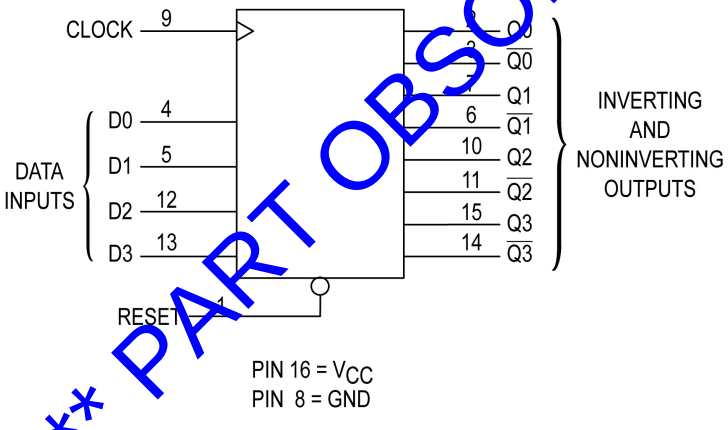
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	RESET	0.122	0.554
2	Q0	0.122	0.251
3	$\overline{Q0}$	0.480	0.122
4	D0	0.780	0.122
5	D1	1.070	0.122
6	$\overline{Q1}$	1.370	0.122
7	Q1	1.771	0.251
8	GND	1.771	0.554
9	CLOCK	1.771	0.781
10	Q2	1.771	1.084
11	$\overline{Q2}$	1.373	1.222
12	D2	1.073	1.222
13	D3	0.783	1.222
14	$\overline{Q3}$	0.483	1.222
15	Q3	0.122	1.084
16	V_{CC}	0.122	0.781
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Truth Table

INPUTS			OUTPUTS	
RESET	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↗	H	H	L
H	↗	L	L	H
H	L	X	No Change	

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC}+1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC}+0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±20	mA
Output Current (per Pad)	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{CC}	2.0	6.0	V
DC Input Voltage, Output Voltage		V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-40	+85	°C
Input Rise / Fall Time	V_{CC}=2.0V	t_r, t_f	0	1000	ns
	V_{CC}=4.5V		0	500	
	V_{CC}=6.0V		0	400	

3. This device contains protection circuitry against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of voltage higher than max rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must be tied to an appropriate logic voltage level (e.g., GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0	V_{OUT} = 0.1V or V_{CC} -0.1V | I_{OUT} | ≤ 20µA	1.5	1.5	1.5	V
		4.5		3.15	3.15	3.15	
		6.0		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0	V_{OUT} = 0.1V or V_{CC} -0.1V | I_{OUT} | ≤ 20µA	0.3	0.3	0.3	V
		4.5		0.9	0.9	0.9	
		6.0		1.2	1.2	1.2	
Minimum High-Level Output Voltage	V_{OH}	2.0	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 20µA	1.9	1.9	1.9	V
		4.5		4.4	4.4	4.4	
		6.0		5.9	5.9	5.9	
		4.5	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 4.0mA	3.98	3.84	3.84	V
		6.0	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 5.2mA	5.48	5.34	5.34	V

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5		0.1	0.1	0.1	
		6.0		0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.33	V
		6.0	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0	V_{IN} = GND or V_{CC}	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0	V_{IN} = GND or V_{DD} I_{OUT} = 0µA	8	80	80	µA

4. -40˚C ≤ T_J ≤ +85˚C

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency (Figure 1, 4)	f_{max}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	6.0	4.8	4.8	MHz
		4.5		30	24	24	
		6.0		35	28	28	
Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1, 4)	t_{PLH}, t_{PHL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	150	190	190	ns
		4.5		30	38	38	
		6.0		26	33	33	
Propagation Delay, Reset to Q or $\overline{Q}$ (Figure 2, 4)	t_{PLH}, t_{PHL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	125	155	155	ns
		4.5		25	31	31	
		6.0		21	26	26	
Output Transition Time, Any Output (Figure 1, 4)	t_{TLH}, t_{THL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	95	ns
		4.5		15	19	19	
		6.0		13	16	16	
Input Capacitance	C_{IN}	-	C_L = 50pF, $t_r = t_f$ = 6ns	10	10	10	pF
Power Dissipation Capacitance (Per Flip-Flop)	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				35			

5. Not production tested in die form, characterized by chip design and tested in package.

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Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, Data to Clock (Figure 3)	t_{su}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	100	125	125	ns
		4.5		20	25	25	
		6.0		17	21	21	
Minimum Hold Time, Clock to Data (Figure 3)	t_h	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	3.0	3.0	3.0	ns
		4.5		3.0	3.0	3.0	
		6.0		3.0	3.0	3.0	
Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	t_{rec}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	100	125	125	ns
		4.5		20	25	25	
		6.0		17	21	21	
Minimum Pulse Width, Clock (Figure 1)	t_w	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	80	100	100	ns
		4.5		16	20	20	
		6.0		14	17	17	
Minimum Pulse Width, Reset (Figure 2)	t_w	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	80	100	100	ns
		4.5		16	20	20	
		6.0		14	17	17	
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	1000	1000	1000	ns
		4.5		500	500	500	
		6.0		400	400	400	

5. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveforms

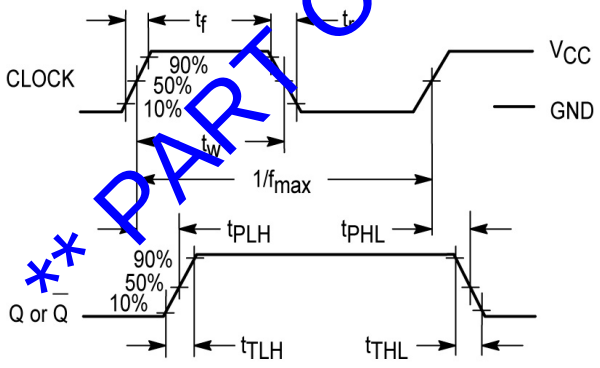


Figure 1 – Data, Clock and Output

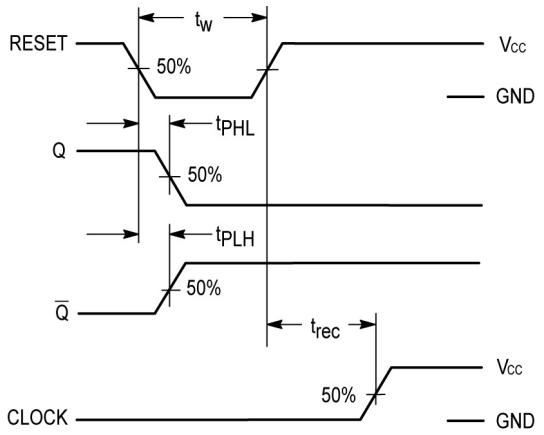


Figure 2 –Reset, Clock and Output

Switching Waveforms continued

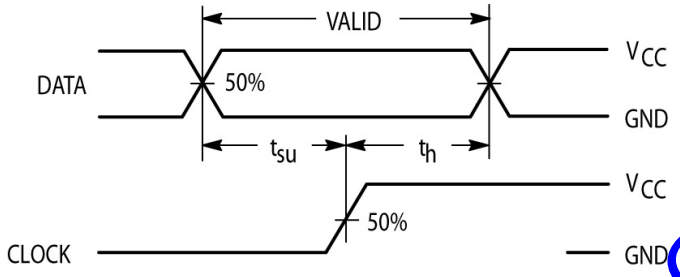
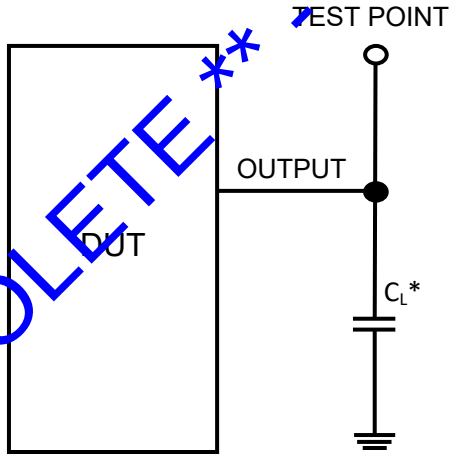


Figure 3 – Clock to Data



* Includes all probe and jig capacitance

Figure 4 – Test Circuit