



High Speed CMOS Logic – 74HC123

Dual re-triggerable monostable multivibrator with reset in bare die form

Rev 1.0
06/10/19

Description

The 74HC123 provides x2 monostable multivibrators each containing two voltage edge trigger inputs, \bar{A} (negative) & B (positive) with Schmitt trigger action providing input tolerance for slow rise/fall timing. An additional trigger function can be executed via a positive edge signal on the Reset pin (\bar{R}). Triggered outputs maintain monostable state for a base time period set by an external resistor Rx & capacitor Cx (see Timing Requirements). Once triggered, the basic output pulse width may be extended by re-triggering \bar{A} or B inputs. A negative edge on Reset breaks monostable state. All unused mono inputs (\bar{A} , B, & \bar{R}) must be set high or low.

Features:

- Triggerable via positive or negative edge
- Re-triggerable for very long pulses up to 100% duty factor
- Direct reset terminates output
- Schmitt trigger action for A & B inputs
- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL.

Ordering Information

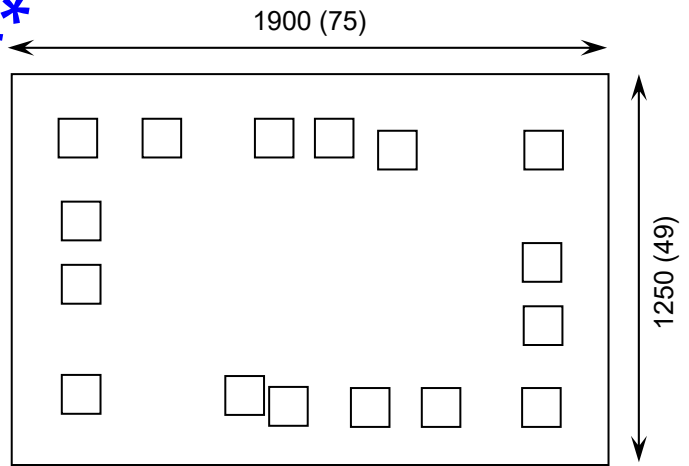
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54HC123](#)

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- ~~Sawn Wafer on Tape – On request~~
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1900 x 1250 75 x 49	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

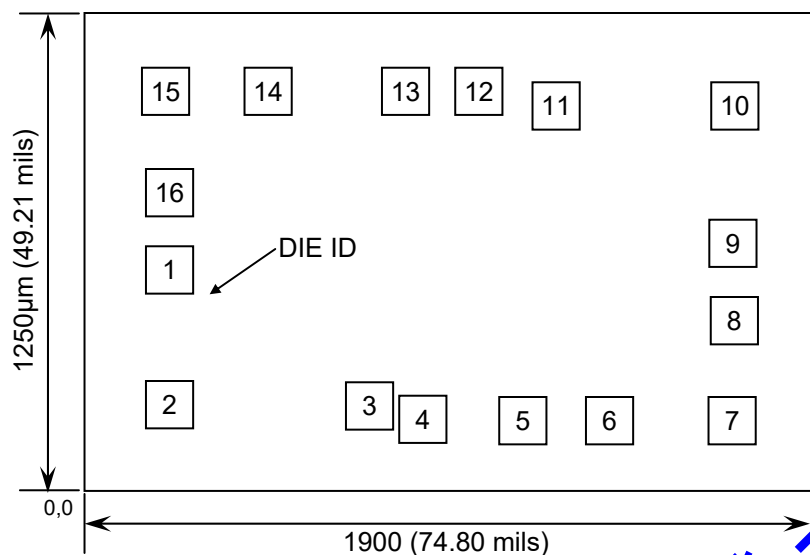




High Speed CMOS Logic – 74HC123

Rev 1.0
06/10/19

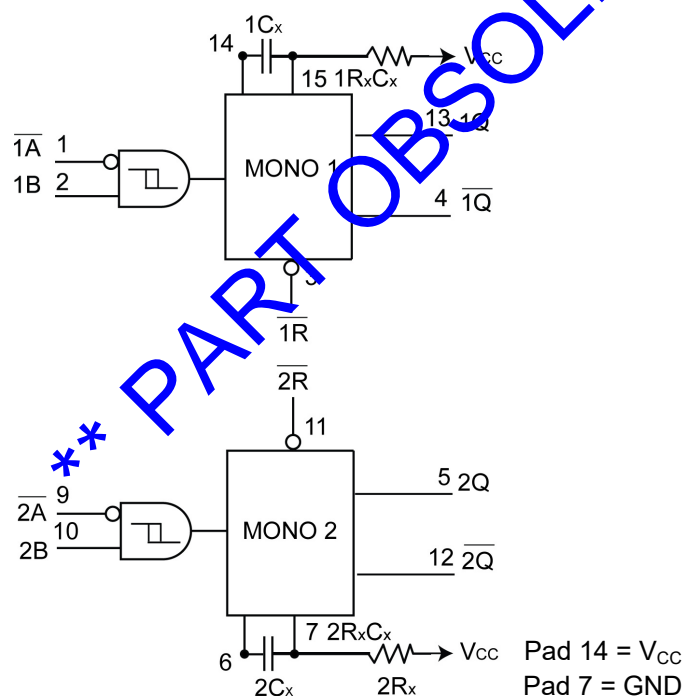
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1A}$	0.155	0.525
2	1B	0.155	0.175
3	$\overline{1R}$	0.680	0.170
4	$\overline{1Q}$	0.815	0.135
5	2Q	1.060	0.130
6	2C _x	1.305	0.130
7	2R _x C _x	1.625	0.135
8	GND	1.625	0.395
9	$\overline{2A}$	1.625	0.595
10	2B	1.625	0.955
11	$\overline{2R}$	1.165	0.955
12	$\overline{2Q}$	0.965	0.995
13	1Q	0.770	0.995
14	1C _x	0.415	0.995
15	1R _x C _x	0.145	0.995
16	V _{CC}	0.155	0.730

CONNECT CHIP BACK TO V_{CC} OR FLOAT

Logic Diagram



Function Table

INPUTS			OUTPUTS		FUNCTION
\overline{A}	B	\overline{R}	Q	\overline{Q}	
↓	H	H			OUTPUT ENABLE
X	L	H	L*	H*	INHIBIT
H	X	H	L*	H*	INHIBIT
L	↑	H			OUTPUT ENABLE
L	H	↑			OUTPUT ENABLE
X	X	L	L	H	INHIBIT

H = High level, L = Low level, X = Don't care,
 ↑ = High-to-low transition, ↓ = Low-to-high transition
 = x1 high level output pulse,
 = x1 low level output pulse
 * If the monostable was triggered before this condition, pulse will continue as programmed.





High Speed CMOS Logic – 74HC123

Rev 1.0

06/10/19

Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to $V_{CC} + 1.5$	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	I_{IN}	\bar{A}, B, \bar{R}	± 20 mA
		C_X, R_X	± 30 mA
DC Output Current, per pad	I_{OUT}	± 25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	± 50	mA
Power Dissipation in Still Air ²	P_D	750	mW
Storage Temperature Range	T_{STG}	-55 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
Supply Voltage	V_{CC}	2	6	V	
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V	
Operating Temperature Range	T_J	-40	+85	°C	
Input Rise or Fall Times - R (Inputs \bar{A} & B are unlimited)	t_r, t_f	$V_{CC} = 2V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6.0V$	0	400	
External Timing Resistor	R_T	$V_{CC} < 4.5V$	10	1000	k Ω
		$V_{CC} > 4.5V$	2	1000	
External Timing Capacitor	C_T	-	No limit	pF	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Input Voltage	V_{IH}	2.0V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT} \leq 20\mu A$	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ $ I_{OUT} \leq 20\mu A$	0.5	0.5	0.5	V
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	





High Speed CMOS Logic – 74HC123

Rev 1.0

06/10/19

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Minimum High-Level Output Voltage	V _{OH}	2.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20μA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 2.4mA	2.48	2.34	2.34	V
		4.5V		3.98	3.84	3.84	
		6.0V		5.48	5.34	5.34	
Maximum Low-Level Output Voltage	V _{OL}	2.0V	V _{IN} = V _{IL} or V _{IL} I _{OUT} ≤ 20μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	V _{IN} = V _{IL} or V _{IL} I _{OUT} ≤ 4.0mA	0.26	0.33	0.33	V
		6.0V		V _{IN} = V _{IL} or V _{IL} I _{OUT} ≤ 5.2mA	0.26	0.33	
Maximum Input Leakage Current	I _{IN}	6.0V	V _{IN} = V _{CC} or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I _{CC}	6.0V	V _{IN} = V _{CC} or GND I _{OUT} = 0μA	130	220	220	μA

4. -40°C ≤ T_J ≤ +85°C

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Propagation Delay, Input A or B to Output Q or Q̄ (Figure 1,2)	t _{PLH} , t _{PHL}	2.0V	C _L = 50pF, t _r = t _f = 6ns	255	320	320	ns
		4.5V		50	65	65	
		6.0V		45	55	55	
Maximum Propagation Delay, Input R to Output Q or Q̄ (Figure 1,2)	t _{PLH} , t _{PHL}	2.0V	C _L = 50pF, t _r = t _f = 6ns	215	270	270	ns
		4.5V		45	55	55	
		6.0V		35	45	45	
Maximum Output Rise and Fall Time, Any Output (Figure 1,2)	t _{TLH} , t _{THL}	2.0V	C _L = 50pF, t _r = t _f = 6ns	75	95	95	ns
		4.5V		16	20	20	
		6.0V		14	17	17	

5. Not production tested in die form, characterized by chip design and tested in package.





High Speed CMOS Logic – 74HC123

Rev 1.0
06/10/19

AC Electrical Characteristics Continued⁵

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁴	
Maximum Input Capacitance	C _{IN}	-	Inputs \bar{A} , B, \bar{R}	10	10	10	pF
			C _X , R _X	25	25	25	
Power Dissipation Capacitance Per Multivibrator ⁶	C _{PD}	-	T _A = 25°C, V _{CC} = 5.0V	TYPICAL			pF
				150			

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Timing Requirements⁵

PARAMETER	SYMBOL	V _{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE ⁵	
Minimum Recovery Time, Reset Inactive to \bar{A} or B (Figure 3)	t _{rec}	2.0V	t _r = t _f = 6ns	50	65	65	ns
		4.5V		10	13	13	
		6.0V		9	11	11	
Minimum Pulse Width, Input \bar{A} or B (Figure 2)	t _w	2.0V	t _r = t _f = 6ns	100	125	125	ns
		4.5V		20	25	25	
		6.0V		17	20	20	
Minimum Pulse Width, R (Figure 3)	t _w	2.0V	t _r = t _f = 6ns	100	125	125	ns
		4.5V		20	25	25	
		6.0V		17	20	20	
Maximum Input Rise and Fall Times, R (Figure 3)	t _r , t _f	2.0V	t _r = t _f = 6ns	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	
Maximum Input Rise and Fall Times, \bar{A} or B (Figure 3)	t _r , t _f	2.0V	t _r = t _f = 6ns	No Limit			ns
		4.5V					
		6.0V					

Timing Requirements - Pulse width formula

When C_X > 10nF and R_X > 10KΩ, the typical output pulse width value is defined by the formula:

$$V_{CC} = 5V, t_w = 0.45 \times R_X \times C_X$$

Where:

t_w = pulse width in ns

R_X = external resistor in kΩ

C_X = external capacitor in pF





High Speed CMOS Logic – 74HC123

Rev 1.0
06/10/19

Switching Waveforms

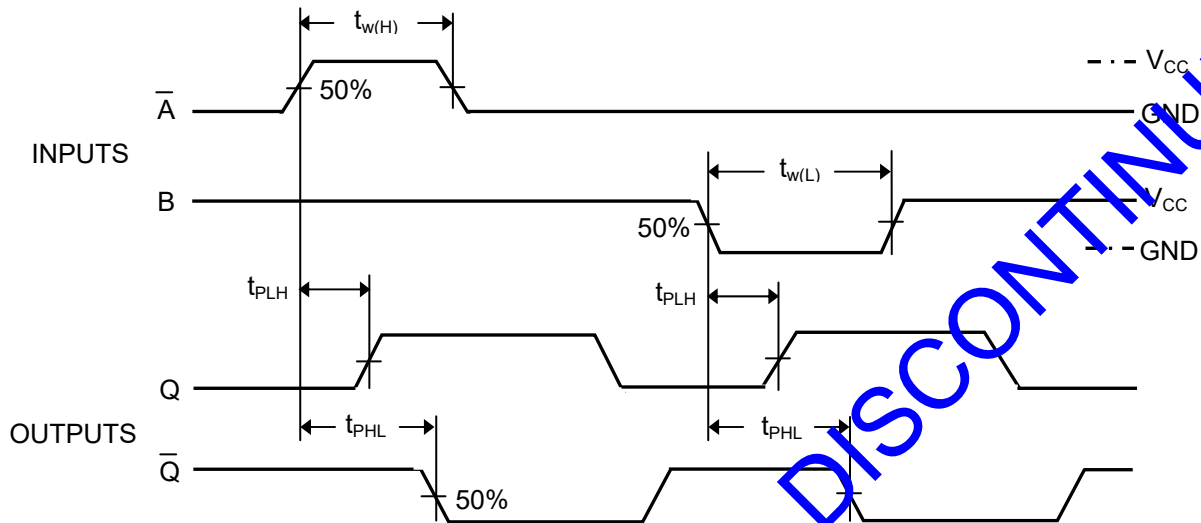


Figure 2 – Propagation Delay & Output Transition Time , Input A or B to Output Q

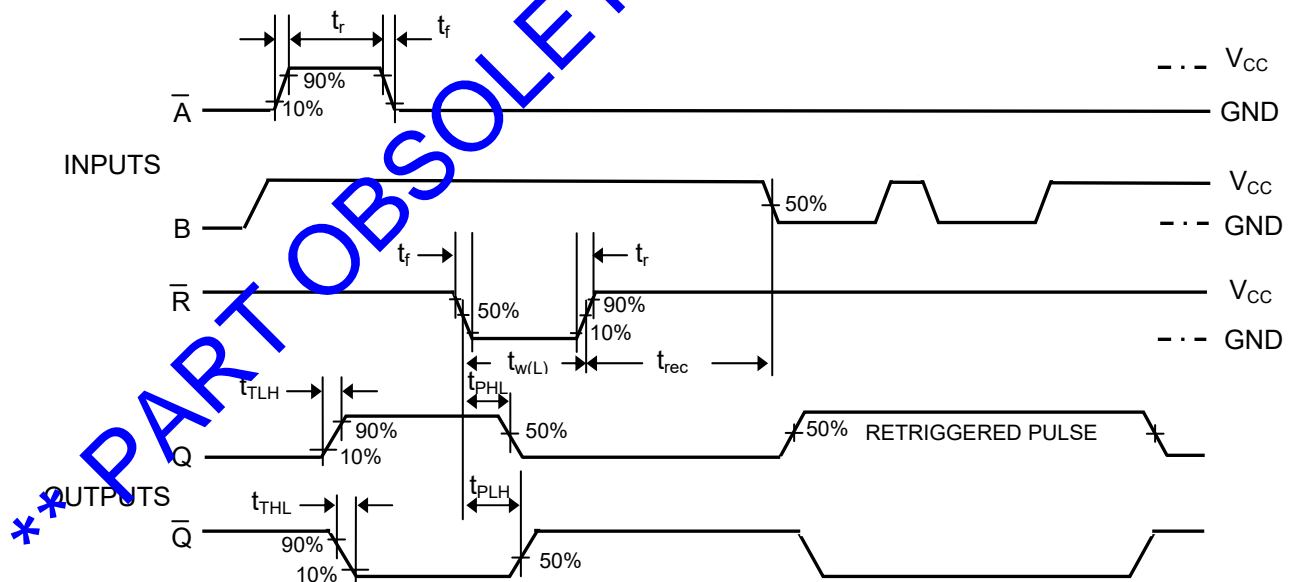


Figure 3 – Propagation Delay & Output Transition Time , Reset to Output with Retrigger

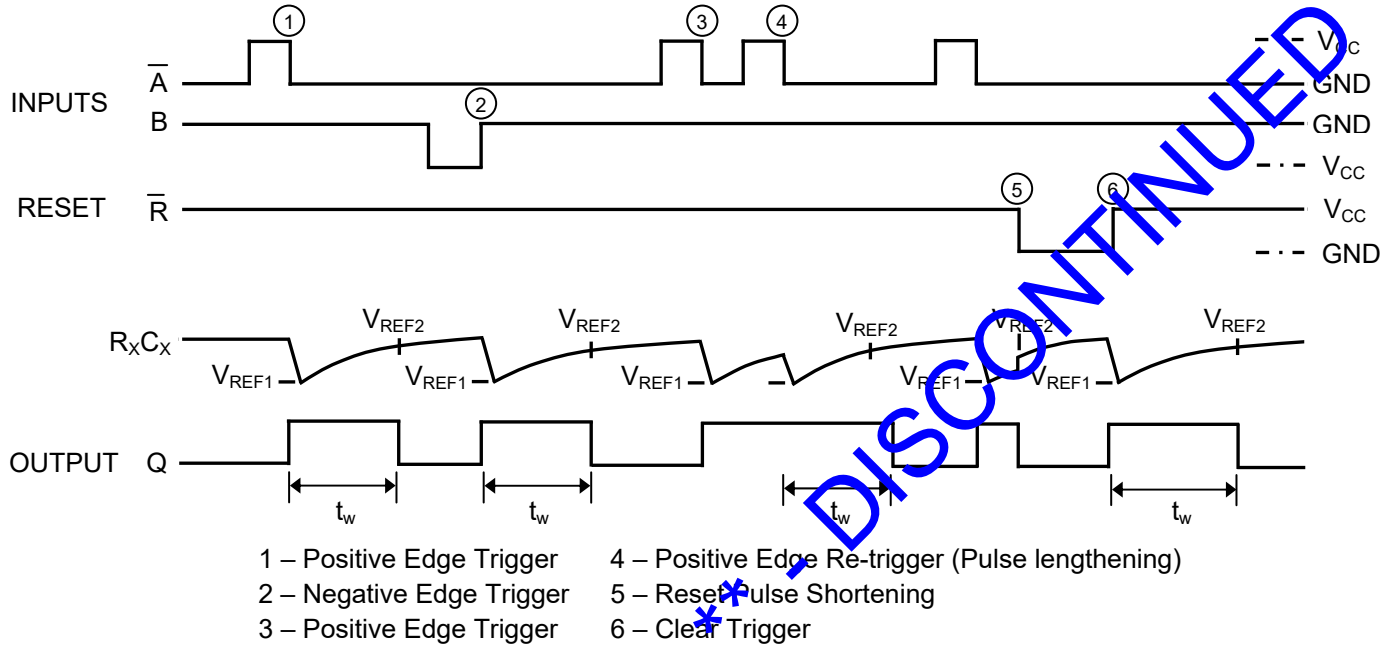




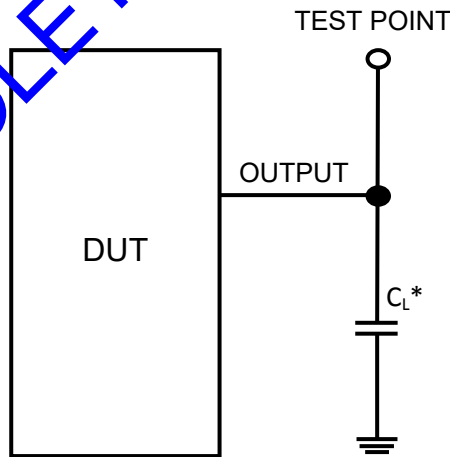
High Speed CMOS Logic – 74HC123

Rev 1.0
06/10/19

Timing Diagram



Test Circuit



* Includes all probe and jig capacitance

DISCLAIMER: The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Silicon Supplies Ltd hereby disclaims any and all warranties and liabilities of any kind.

LIFE SUPPORT POLICY: Silicon Supplies Ltd components may be used in life support devices or systems only with the express written approval of Silicon Supplies Ltd, if a failure of such components can reasonably be expected to cause the failure of that life support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

