High Speed CMOS Logic – 74HC112

Dual J-K Flip-Flops with preset and clear; negative edge trigger in bare die form

Rev 1.0
24/11/17

Description

The 74HC112 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. Each flip-flop has independent J, K, preset, clear, clock inputs and Q $\overline{Q}$ outputs. A high level at the clock input enables the J and K inputs to accept data. The device changes state on the negative going transition of the clock pulse. Preset and clear are independent of the clock and are accomplished by a low logic level on the corresponding input. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Bus Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS112.

Ordering Information

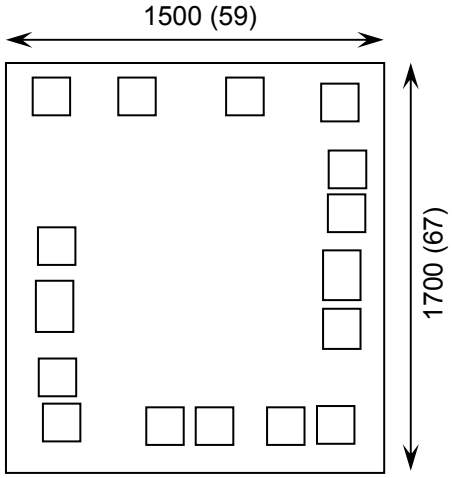
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability version of this product please see

54HC112

Die Dimensions in µm (mils)



Supply Formats:

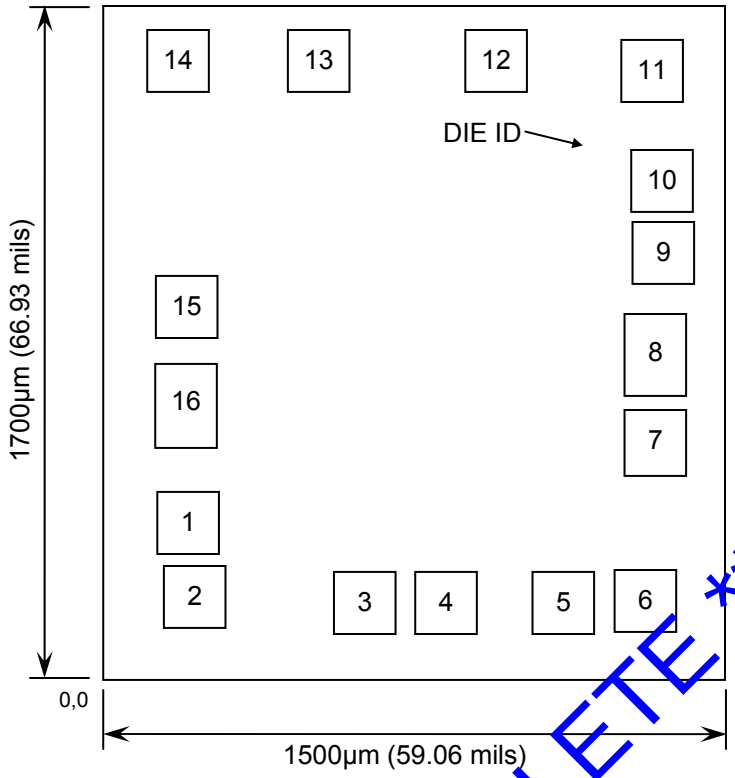
- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1500 x 1700 59 x 67	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Rev 1.0
24/11/17

Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$1\overline{CLK}$	0.125	0.345
2	1K	0.135	0.125
3	1J	0.585	0.135
4	$1\overline{PRE}$	0.755	0.135
5	1Q	1.025	0.135
6	$1\overline{Q}$	1.225	0.135
7	$2\overline{Q}$	1.245	0.54
8	GND	1.245	0.735
9	2Q	1.26	0.995
10	$2\overline{PRE}$	1.26	1.165
11	2J	1.25	1.47
12	2K	0.86	1.48
13	$2\overline{CLK}$	0.48	1.48
14	$2\overline{CLR}$	0.125	1.47
15	$1\overline{CLR}$	0.125	0.855
16	V_{CC}	0.125	0.615
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

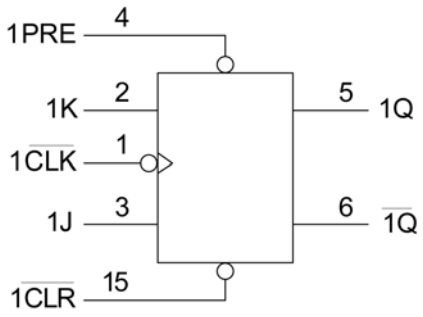
Truth Table

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	$\overline{CLK}$	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	NO CHANGE	
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	NO CHANGE	

H = High level (steady state), L = Low level (steady state)
X = Don't care, ↓ = High-to-Low transition

* Output states unpredictable if both PRE and CLR go High simultaneously after both being low at the same time.

Logic Diagram



x1 Flip-Flop

Rev 1.0
24/11/17

Pad Descriptions

CLOCK INPUTS
1$\overline{CLK}$, 2$\overline{CLK}$ (Pads 1, 13)
Clock input (HIGH-to-LOW, edge triggered)

DATA INPUTS
1K, 2K, 1J, 2J (Pads 2, 12, 3, 11)
Data inputs; flip-flops 1 and 2

OUTPUTS
1Q, 2Q, 1$\overline{Q}$, 2$\overline{Q}$ (Pads 5, 9, 6, 7)
True flip-flop outputs and complement flip-flop outputs

CONTROL INPUTS
1$\overline{PRE}$, 2$\overline{PRE}$ (Pads 4, 10)
Set inputs (active LOW)
1$\overline{CLR}$, 2$\overline{CLR}$ (Pads 15, 14)
Reset inputs (active LOW)

GROUND & POWER
GND, V_{CC} (Pads 8, 16)
Ground 0V, Positive Supply Voltage

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum ratings may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	0	+85	°C
Input Rise and Fall Time	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert \le 20\mu A$	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert \le 20\mu A$	0.3	0.3	0.3	V
		4.5V		0.9	0.9	0.9	
		6.0V		1.2	1.2	1.2	
Minimum High-Level Output Voltage	V_{OH}	2.0V	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert \le 20\mu A$	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		4.5V	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT} \rvert \le 4.0mA$	3.98	3.84	3.84	
		6.0V	V_{IN} = V_{IH} $\lvert I_{OUT} \rvert \le 5.2mA$	5.48	5.34	5.34	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	V_{IN} = V_{IL} or V_{IH} $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH} $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.33	
		6.0V	V_{IN} = V_{IL} or V_{IH} $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	4	40	40	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Max Clock Frequency, 50% Duty Cycle (Figure 1, 4)	f_{max}	2.0V	C_L = 50pF, t_r = t_f = 6ns	6.0	4.8	4.8	MHz
		4.5V		30	24	24	
		6.0V		35	28	28	
Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1, 4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, t_r = t_f = 6ns	125	155	155	ns
		4.5V		25	31	31	
		6.0V		21	36	36	
Maximum Propagation Delay, Reset to Q or $\overline{Q}$ (Figure 2,4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, t_r = t_f = 6ns	155	195	195	ns
		4.5V		31	39	39	
		6.0V		26	33	33	

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Set to Q or ~~Q~~ (Figure 2,4)	t_{PLH}, t_{PHL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	165	205	205	ns
		4.5V		33	41	41	
		6.0V		28	35	35	
Maximum Output Transition time, Any output (Figure 1,4)	t_{TLH}, t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	95	ns
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance[6] (Per Flip-Flop)	C_{PD}	-	-	TYPICAL			pF
				35			

Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Setup Time, J or K to Clock (Figure 3)	t_{SU}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	100	125	125	ns
		4.5V		20	25	25	
		6.0V		17	21	21	
Minimum Hold Time, Clock to J or K (Figure 3)	t_h	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	3	3	3	ns
		4.5V		3	3	3	
		6.0V		3	3	3	
Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	t_{rec}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	100	125	125	ns
		4.5V		20	25	25	
		6.0V		17	21	21	
Minimum Pulse Width, Clock (Figure 1)	t_w	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	80	100	100	ns
		4.5V		16	20	20	
		6.0V		14	17	17	
Minimum Pulse Width, Set or Reset (Figure 2)	t_w	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	80	100	100	ns
		4.5V		16	20	20	
		6.0V		14	17	17	
Maximum Input Rise and Fall times (Figure 1)	t_r, t_f	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	1000	1000	1000	ns
		4.5V		500	500	500	
		6.0V		400	400	400	

4. $0^{\circ}C \le T_J \le +85^{\circ}C$

5. Not production tested in die form, characterized by chip design and tested in package.

6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Rev 1.0
24/11/17

Switching Waveforms

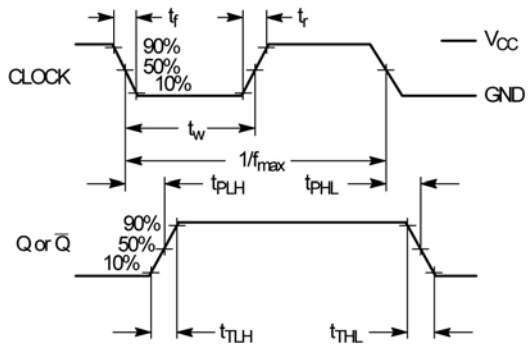


Figure 1 – Propagation Delay & Output transition

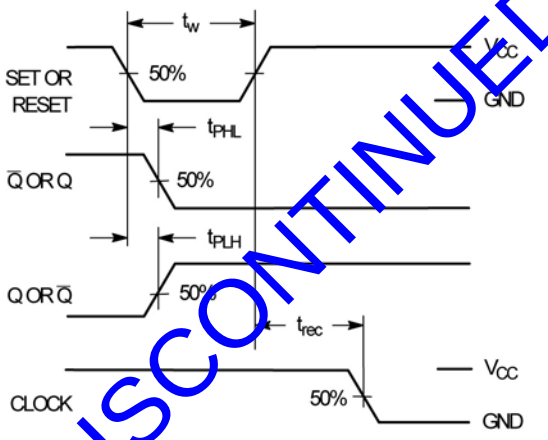


Figure 2 – Propagation Delay, Pulse Width & Recovery

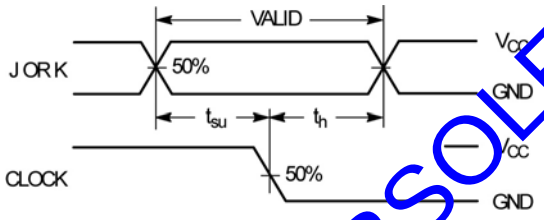
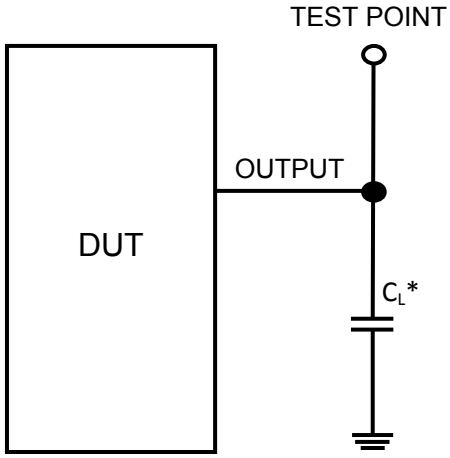


Figure 3 – Setup & Hold time

Test Circuits



* Includes all probe and jig capacitance

Figure 4