

Quad 2-Input Open Drain NAND Gate in bare die form

Rev 1.0 16/04/18

Description

The 74HC03 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. This device is comprised of 3 stages including buffer output, which enables high noise immunity with stable output. With an external pull-up resistor the device can be used in wired AND configuration. This device can be also used as an LED driver and in any other application requiring a current sink. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{\rm CC}$ and Ground.

Features:

- Output Drive Capability: 10 LSTTL Lyads
- Low Input Current: 1µA
- Outputs directly interface CNCS NMOS and TTL
- Operating Voltage Range: 2% to 6V
- CMOS High Noise Impunity
- Function compatible with 74LS03.

Ordering Information

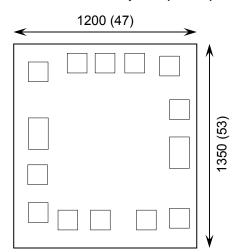
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection,

For High Reliability versions of this product please see

54HC03

Die Dimensions in µm (mils)



Supply Formats:

- Defaut Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

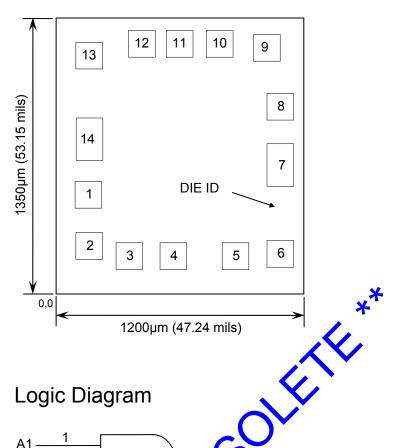
Die Size (Unsawn)	1200 x 1350 47 x 53	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	μm mils
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1μ	m
Back Metal Composition	N/A – Bare S	Si





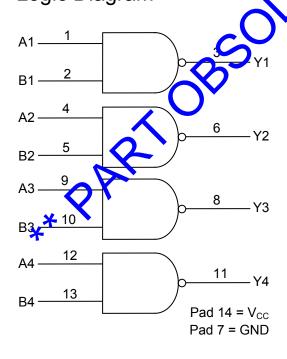
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Pad Layout and Functions



PAD	FUNCTION	COORDINA	115 (mm)
FAD	FUNCTION	Х	Y
1	A1	0.131	0.460
2	B1	0.131	0.153
3	Y1	0.305	0.121
4	A	0.489	0.121
5	B2	0.786	0.121
6	1 2	0.970	0.131
70	GND	0.980	0.462
2	Y3	0.980	0.764
Э	А3	0.950	1.115
10	В3	0.713	1.125
11	Y4	0.543	1.125
12	A4	0.369	1.125
13	B4	0.131	1.091
14	V _{CC}	0.131	0.631
CON	NECT CHIP BA	CK TO V _{CC} O	R FLOAT

Logic Diagram



Truth Table

INPU	JTS	OUTPUT
Α	В	Υ
L L	L H	Z Z 7
H	Н	L

H = High level (steady state) L = Low level (steady state)

Z = High Impedance state



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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-1.5 to V _{CC} +1.5	Y ,
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	
DC Input Current, per pin	I _{IN}	±20	mA
DC Output Current, per pin	I _{OUT}	±25	mA
DC V _{CC} or GND Current, per pin	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 (0 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die at ach and assembly method.

Recommended Operating Conditions³ (Voltages refurenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	V _{CC}	x 2	6	V	
DC Input or Output Voltage	V_{IN} , V_{OUT}	* 0	V _{CC}	V	
Operating Temperature Ran	T _J	0	+85	°C	
	V _{CC} = 2.0V		/ 0	1000	
Input Rise and Fall Time	$V_{CC} = 4.5V$	t_r , t_f	0	500	ns
		0	400		

^{3.} This device contains protection circuitry to guard gainst damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than naximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND \leq (V_{IN} or V_{CC}). Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	V _{CC} CONDITIONS LIMITS	V _{2.2} CONDITIONS LIMITS	LIMITS			ONDITIONS	CONDITIONS	3	UNITS
		V CC	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS V V				
Minimum High I		2.0V	V _{OUT} = 0.1V or	1.5	1.5	1.5					
Minimum High Level Input Voltage	V_{IH}	4.5V	V _{CC} -0.1V	3.15	3.15	3.15	V				
mpat votego		$ I_{OUT} \le 20 \mu A$	4.2	4.2	4.2						
Maying Law Lavel		2.0V	V _{OUT} = 0.1V or	0.5	0.5	0.5					
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V _{CC} -0.1V	1.35	1.35	1.35	V				
		6.0V	I _{OUT} ≤ 20μA	1.8	1.8	1.8					

^{4.} $0^{\circ}C \le T_{J} \le +85^{\circ}C$





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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS	LIMITS			UNITS
TAIVAMETER	OTHEOL	• 66	CONDITIONS	25°C	85°C	FULL RANGE	
		2.0V	\/ - \/	0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ $\left I_{OUT} \right \le 20 \mu A$	0.1	0.1	0.1	
Maximum Low-Level Output Voltage	.,	6.0V	1.0011 = 15.	0.1	0.1		
	V _{OL}	4.5V	$\begin{vmatrix} V_{\text{IN}} = V_{\text{IH}} \\ \left I_{\text{OUT}} \right \le 4.0 \text{mA} \end{vmatrix}$	0.26	0.33	0.53	V
		6.0V	$\begin{vmatrix} V_{\text{IN}} = V_{\text{IH}} \\ \left I_{\text{OUT}} \right \le 5.2 \text{mA} \end{vmatrix}$	0.26	0.32	0.33	
Maximum Input Leakage Current	I _{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum 3-State leakage current	I _{OZ}	6.0V	$V_{OUT}=V_{CC}$ or GND $V_{IN}=V_{IL}$ or V_{IH}	±0:5	±5.0	±5.0	μA
Maximum Quiescent Supply Leakage Current	I _{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$		10	10	μА

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIMITS		UNITS
	O I MIDOL	· cc	COUDITIONS	25°C	85°C	FULL RANGE⁴	Sittio
Maximum		2.0V		120	150	150	
Propagation Delay,	t _{PLZ} , t _{PZL}	4.50	$C_L = 50pF,$ $t_r = t_f = 6ns$	24	30	30	ns
A or B to Y (Figures 2,4)	C	9.0V	ι _r – ι _f – 0115	20	26	26	
Maximum	(h)	2.0V		75	95	95	
Output Transition Time,	TH.	4.5V	$C_L = 50pF,$ $t_r = t_f = 6ns$	15	19	19	ns
any Output (Figures 2,4)	O	6.0V		13	16	16	
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Maximum Three-State Output Capa itance (Output in High- Impedance State)	Соит	-	-	10	10	10	pF
Power Dissipation			T _A = 25°C,	TYPICAL			pF
Capacitance (Per Gate) ⁶	C _{PD}	-	$V_{CC} = 5.0V$		8		рг

^{5.} Not production tested in die form, characterized by chip design and tested in package LAT.



^{6.} Used to determine the no-load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$.



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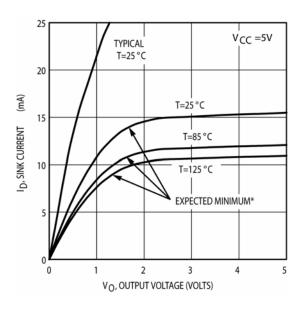
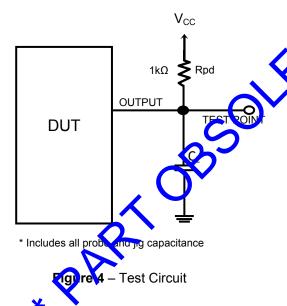


Figure 1 - Open-Drain Output Characteristics



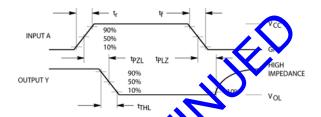


Figure 2 - Switching Waveforms

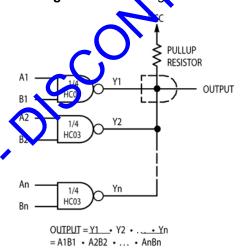


Figure 3 - Wired AND

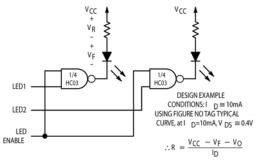


Figure 5 – LED Driver with blanking

 $= \frac{5V - 1.7V - 0.4V}{10\text{mA}}$ $= 290 \Omega$ $USE R = 270 \Omega$

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