High Speed CMOS Logic – 74HC03

Quad 2-Input Open Drain NAND Gate in bare die form

Rev 1.0
16/04/18

Description

The 74HC03 is fabricated using a 2.5µm 5V CMOS process and has the same high speed performance of LSTTL combined with CMOS low power consumption. This device is comprised of 3 stages including buffer output, which enables high noise immunity with stable output. With an external pull-up resistor the device can be used in wired AND configuration. This device can be also used as an LED driver and in any other application requiring a current sink. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and Ground.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- CMOS High Noise Immunity
- Function compatible with 74LS03.

Ordering Information

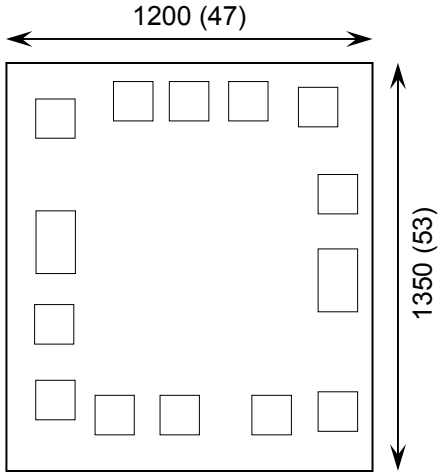
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54HC03

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1200 x 1350 47 x 53	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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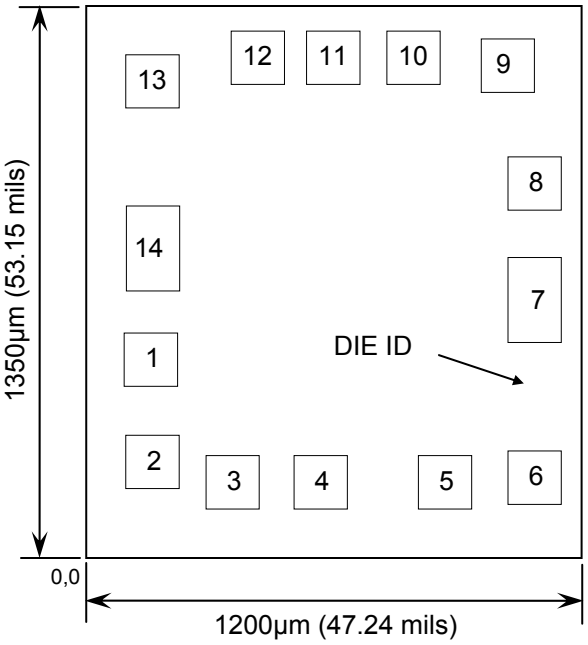
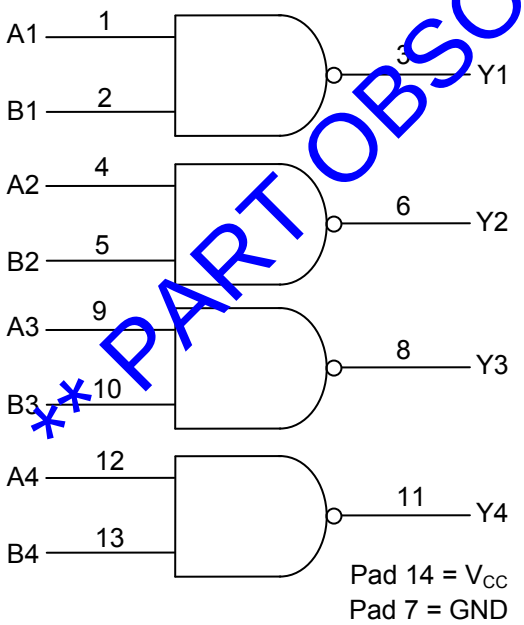
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A1	0.131	0.460
2	B1	0.131	0.153
3	Y1	0.305	0.121
4	A2	0.489	0.121
5	B2	0.786	0.121
6	Y2	0.970	0.131
7	GND	0.980	0.462
8	Y3	0.980	0.764
9	A3	0.950	1.115
10	B3	0.713	1.125
11	Y4	0.543	1.125
12	A4	0.369	1.125
13	B4	0.131	1.091
14	V_{CC}	0.131	0.631
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance state

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-1.5 to V_{CC} +1.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pin	I_{IN}	±20	mA
DC Output Current, per pin	I_{OUT}	±25	mA
DC V_{CC} or GND Current, per pin	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	2	6	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	0	+85	°C
Input Rise and Fall Time	V_{CC} = 2.0V	t_r, t_f	0	1000	ns
	V_{CC} = 4.5V		0	500	
	V_{CC} = 6.0V		0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert \le$ 20µA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert \le$ 20µA	0.5	0.5	0.5	V
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

4. 0°C ≤ T_J ≤ +85°C

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DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IH}$ $\lvert I_{OUT} \rvert \le 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IH}$ $\lvert I_{OUT} \rvert \le 4.0mA$	0.26	0.33	0.33	
		6.0V	$V_{IN} = V_{IH}$ $\lvert I_{OUT} \rvert \le 5.2mA$	0.26	0.33	0.33	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State leakage current	I_{OZ}	6.0V	$V_{OUT}=V_{CC}$ or GND $V_{IN} = V_{IL}$ or V_{IH}	±0.5	±5.0	±5.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	10	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, A or B to Y (Figures 2,4)	t_{PLZ}, t_{PZL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	120	150	150	ns
		4.5V		24	30	30	
		6.0V		20	26	26	
Maximum Output Transition Time, any Output (Figures 2,4)	t_{THL}	2.0V	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	95	ns
		4.5V		15	19	19	
		6.0V		13	16	16	
Maximum Input Capacitance	C_{IN}	-	-	10	10	10	pF
Maximum Three-State Output Capacitance (Output in High-Impedance State)	C_{OUT}	-	-	10	10	10	pF
Power Dissipation Capacitance (Per Gate)[6]	C_{PD}	-	T_A = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				8			

5. Not production tested in die form, characterized by chip design and tested in package LAT.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

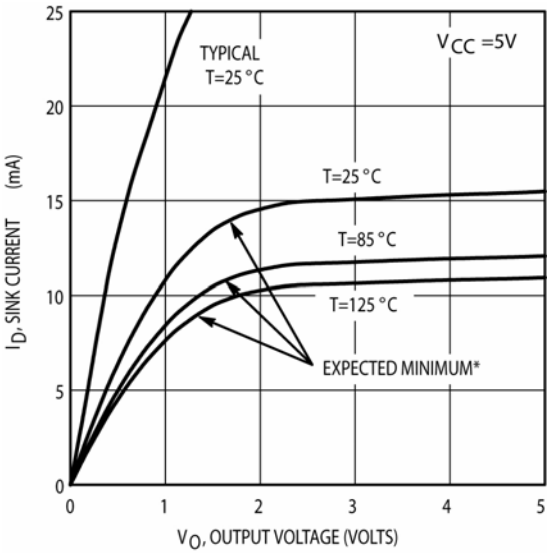


Figure 1 – Open-Drain Output Characteristics

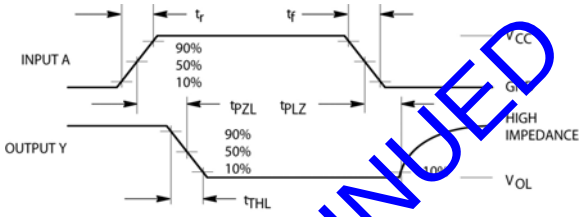


Figure 2 – Switching Waveforms

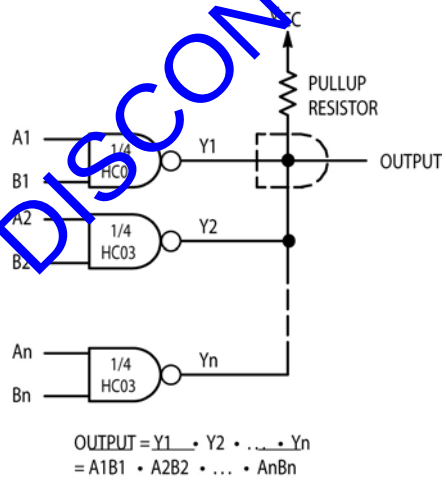
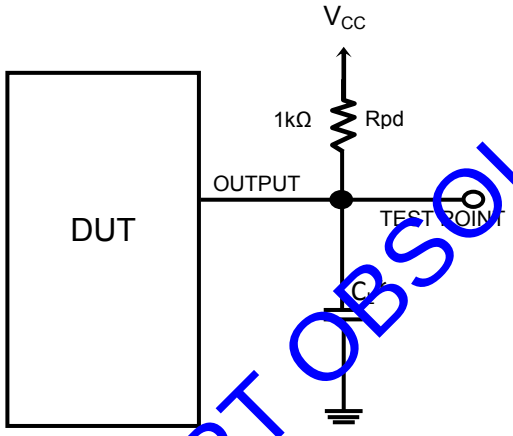


Figure 3 – Wired AND



* Includes all probe and jig capacitance

Figure 4 – Test Circuit

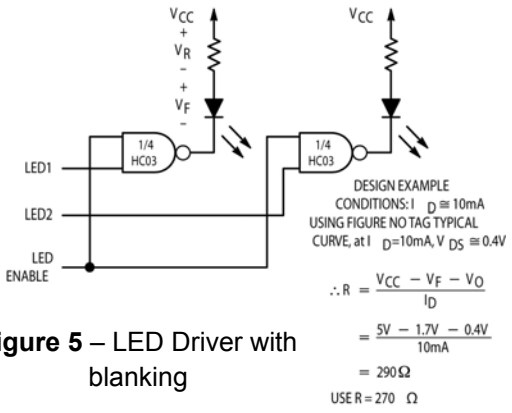


Figure 5 – LED Driver with blanking