

4-bit Binary Counter Logic IC in bare die form

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Description

The 74ALS93 4-bit binary counter is fabricated using a 2µm 40V bipolar process. The device comprises two 4-bit ripple type counters consisting of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has independent clock (CK) & asynchronous master reset (R0) inputs. Counter state change is triggered by a high-to-low transition on the clock. Each section can be used separately or tied together (Q to CK) to form BCD or modulo-16 counters.

Features:

- Low Power Consumption
- Input Clamp Diodes Limit High Speed Termination Effects
- Direct drop-in replacement for obsolete components in long term programs.

Ordering Information

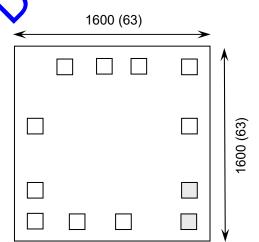
The following part suffixes apply:

No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ALS93

Die Dimensions in µm (mils)



Supply Formats:

- Defaut Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Mechanical Specification

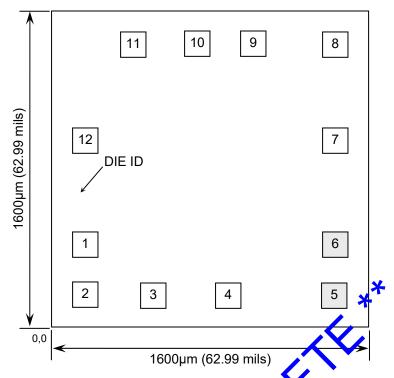
Die Size (Unsawn)	1600 x 1600 63 x 63	µm mils	
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils	
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils	
Top Metal Composition	Al 1%Si 1.1μ	m	
Back Metal Composition	N/A – Bare Si		





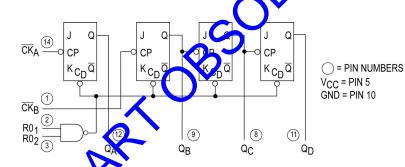
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Pad Layout and Functions



			\leftarrow
PAD	FUNCTION	COORDIN	ATES (mm)
FAD	FUNCTION	Х	Y
1	CK _B	0.100	0.360
2	R0 ₍₁₎	0.100	0.100
3	R0 ₍₂₎	0.450	0.100
4	Vo	0.830	0.100
5	NO	1.370	0.100
6	NC	1.370	0.360
_TC	Q _C	1.370	0.880
2	Q _B	1.370	1.370
Э	GND	0.960	1.370
10	Q_D	0.670	1.370
11	Q _A	0.350	1.370
12	CK _A	0.100	0.880
	CONNECT CHI	P BACK TO	GND

Logic Diagram



Truth Table

COUNT	OUTPUT					
COOM	Q _A	Q _B	Q _C	Q_D		
0	L	L	L	L		
1	H	L	L	L		
2	L	H	L	L		
3	H	H	L	L		
4	L	L	H	L		
5	Н	L	H	L		
6	L	H	H	L		
7	H	H	H	L		
8	L	L	L	Н		
9	Н	L	L	Н		
10	L	H	L	Н		
11	Н	H	L	Н		
12	L	L	H	Н		
13	Н	L	H	Н		
14	L	H	H	Н		
15	Н	Н	Н	Н		
NOTE: OUTPUT QA IS CONNECTED TO INPUT CKB						
H = HIGH Voltage Level L = LOW Voltage Level						

Mode Selection

X RESET	INPUT	OUTPUT				
R0 ₍₁₎	R0 ₍₂₎	Q_A	Q_B	Q_{C}	Q_D	
Н	Н	L	L	L	L	
L	Н	COUNT				
Н	L	COUNT				
L	L	COUNT				



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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	7.0	
Storage Temperature Range	T _{STG}	-65 to 150	~

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

1 5							
PARAMETER	SYMBOL	MIN	MAX	STIND			
Supply Voltage (Referenced to GND)	V _{CC}	4.75	5.25				
High-Level Input Voltage	V _{IH}	2	~	V			
Low-Level Input Voltage	V _{IL}	-	0.8	V			
High-Level Output Current	I _{OH}	-	-0.4	mA			
Low-Level Output Current	I _{OL}	-	8	mA			
Operating Temperature Range	T _J	-40 🥕	+85	°C			
Operating Temperature Range	T _J	-40	+85	°C			

DC Electrical Characteristics Voltage's referenced to GND, T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL CONDITIONS	LIMITS			UNITS	
FARAWILTER	STWIDOL	CONDITIONS	MIN	TYP	MAX	ONITS
Minimum High-Level Input Voltage	V _{IH}	0	2	-	-	V
Maximum Low-Level Input Voltage	V _{IL}	-	-	-	0.8	V
Input Clamp Diode Voltage		$V_{CC} = 4.5V$ $I_{IN} = -18mA$	-	-0.65	-1.5	V
Output Voltage High	V _{OH}	$V_{CC} = 4.5V, I_{OH} = -0.4mA$	V _{CC} -2	-	-	V
Output Voltage Lw	V _{OL}	V _{CC} = 4.5V, I _{OL} = 4mA	-	0.25	0.4	V
odipat Volido 24.		$V_{CC} = 4.5V, I_{OL} = 8mA$	-	0.35	0.5	
Inp High Current	ı	$V_{CC} = 5.5V, V_{IN} = 2.7V$	-	-	20	μA
inpat night Current	I _{IH}	$V_{CC} = 5.5V, V_{IN} = 7.0V$	-	-	0.1	mA
Input Low Current	I _{IL}	$V_{CC} = 5.5V, V_{IL} = 0.4V$	-	-	-0.1	mA
Short Circuit Current ²	I _{os}	$V_{CC} = 5.5V, V_{OUT} = 2.25V$	-30	-	-112	mA
Supply Current	I _{CC}	V _{CC} = 5.5V	-	-	13	mA

^{2.} Not more than one output should be shorted at a time, nor for more than 1 second.





AC Electrical Characteristics 4 V_{CC} = 5V, T_J = -40°C to 85°C unless otherwise specified

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PARAMETER	SYMBOL CONDITIONS		LIMITS			DNITS
TANAMETER	OTHIBOL		MIN	TYP	MAX	
Input Clock Frequency, CK _A	f _{max}		32	-	-	MHz
Input Clock Frequency, CK _B	max	$C_L = 50 pF, R_L = 510 \Omega$	16	-		MHz
Fall, Rising Edge	t _f , t _r		-	-	2	ns
Propagation Delay, CK_A to Q_A	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	4	16	ns
Propagation Delay, CK_A to Q_A	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	~ <u>O</u> `	18	113
Propagation Delay, CK_A to Q_D	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-, C	9 .	70	ns
Propagation Delay, CK_A to Q_D	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$		-	70	ns
Propagation Delay, CK_B to Q_B	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	16	ns
Propagation Delay, CK_B to Q_B	t _{PHL}	$C_L = 50 \text{pF}, R_L = 510 \Omega$	-	-	21	ns
Propagation Delay, CK_B to Q_C	t _{PLH}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	32	ns
Propagation Delay, CK_B to Q_C	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	35	ns
Propagation Delay, CK_B to Q_D	t _{PLH}	$_{L}$ = 50pF, R _L = 510Ω	-	-	51	ns
Propagation Delay, CK_B to Q_D	PHL	$C_L = 50 pF, R_L = 510 \Omega$	-	-	51	ns
Propagation Delay, R0 to any output	t _{PHL}	$C_L = 50 pF, R_L = 510 \Omega$	-	-	32	ns

Timing Requirements⁴ V_{CC} = 5V, T_J = -40°C to 85°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		LIMITS		UNITS
*	O'IIIBOL		MIN	TYP	MAX	J. G.
CK _A Pulse Width		$C_L = 50pF, R_L = 510\Omega$	15	-	-	ns
CK _B Pulse Width	t _W		30	-	-	ns
R0 Pulse Width			15	-	-	ns
Recovery Time, R0 to CK	t _{REC}	$C_L = 50 pF, R_L = 510 \Omega$	25	-	-	ns

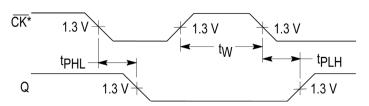
^{4.} Not production tested in die form, characterized by chip design.



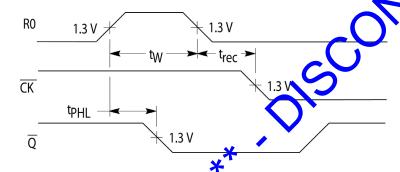


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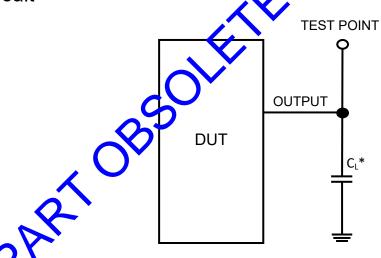
Switching Waveforms



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the Truth Table



Test Circuit



* Includes all probe and jig capacitance

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