



# Advanced Low Power Schottky Logic – 74ALS86

Quadruple 2-Input Exclusive OR Gate IC in bare die form

Rev 1.0  
01/11/22

## Description

The 74ALS86 is fabricated using a 1.5µm 40V Bipolar process. The device contains four independent gates and performs the Boolean functions  $Y = A \oplus B = \bar{A}B + A\bar{B}$  in positive logic.

## Features:

- High speed – 3ns (Min) propagation delay
- Direct drop-in replacement for obsolete components in long term programs.

## Ordering Information

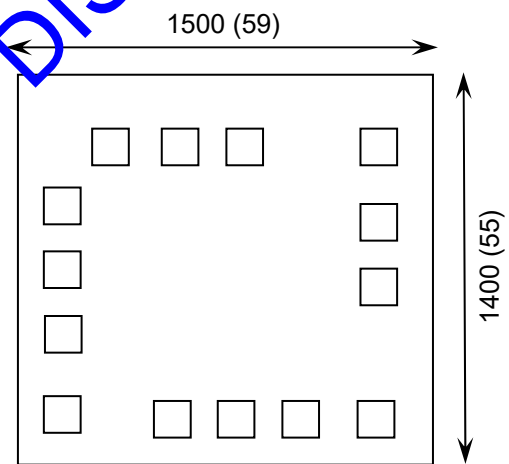
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54ALS86](#)

## Die Dimensions in µm (mils)



## Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- ~~Sawn~~ Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

## Mechanical Specification

Die Size (Unsawn)	1500 x 1400 59 x 55	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

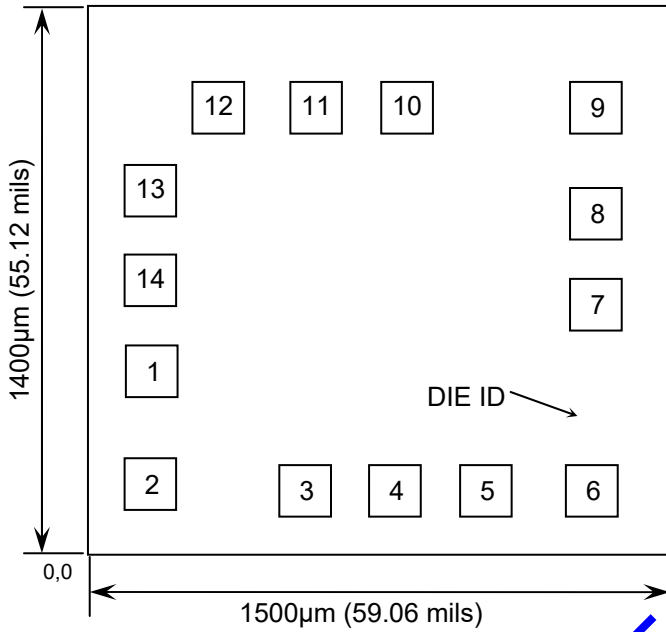




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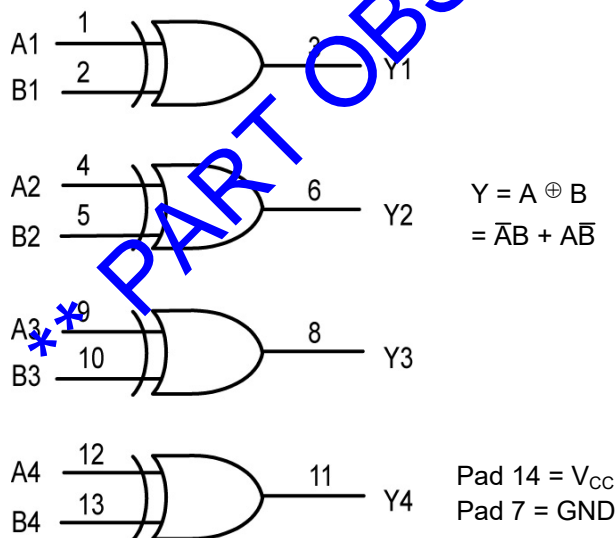
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.100	0.405
2	1B	0.100	0.175
3	1Y	0.495	0.100
4	2A	0.725	0.100
5	2B	0.955	0.100
6	2Y	1.245	0.100
7	GND	1.235	0.575
8	3Y	1.235	0.805
9	3A	1.235	1.075
10	3B	0.753	1.075
11	4Y	0.525	1.075
12	4A	0.270	1.075
13	4B	0.100	0.865
14	V <sub>CC</sub>	0.100	0.635

CONNECT CHIP BACK TO GND

## Logic Diagram



## Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High level (steady state)  
L = Low level (steady state)





## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	$V_{CC}$	7.0	V
DC Input Voltage	$V_{IN}$	7.0	V
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

## Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{CC}$	4.5	5.5	V
High-Level Input Voltage	$V_{IH}$	2	-	V
Low-Level Input Voltage	$V_{IL}$	-	0.8	V
High-Level Output Current	$I_{OH}$	-	-0.4	mA
Low-Level Output Current	$I_{OL}$	-	8	mA
Operating Temperature Range	$T_J$	-40	+85	°C

## DC Electrical Characteristics<sup>2</sup> $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Minimum High-Level Input Voltage	$V_{IH}$	-	2	-	-	V	
Maximum Low-Level Input Voltage	$V_{IL}$	-	-	-	0.8	V	
Input Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{MIN}$ $I_{IN} = -18\text{mA}$	-	-	-1.5	V	
Output Voltage High	$V_{OH}$	$V_{CC} = 4.5\text{V to } 5.5\text{V}$ , $I_{OH} = -0.4\text{mA}$	$V_{CC} - 2$	-	-	V	
Output Voltage Low	$V_{OL}$	$V_{CC} = 4.5\text{V}$	$I_{OL} = 4\text{mA}$	-	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	-	0.35	0.5	
Input Current	$I_{IN}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 7\text{V}$	-	-	0.1	mA	
Input High Current	$I_{IH}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 2.7\text{V}$	-	-	20	$\mu\text{A}$	
Input Low Current	$I_{IL}$	$V_{CC} = 5.5$ , $V_{IN} = 0.4\text{V}$	-	-	-0.1	mA	
Output Current <sup>3</sup>	$I_O$	$V_{CC} = 5.5$ , $V_{OUT} = 2.25\text{V}$	-30	-	-112	mA	
Power Supply Current	$I_{CC}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 4.5\text{V}$ (All inputs)	-	3.9	5.9	mA	

2. All typical values @  $V_{CC} = 5\text{V}$ ,  $T_J = 25^{\circ}\text{C}$ .

3. Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$





## AC Electrical Characteristics<sup>4</sup> $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, A or B to output Y (other input low)	$t_{PLH}$	$V_{CC} = 4.5$ to $5.5\text{V}$ , $C_L = 50\text{pF}$ , $R_L = 500\Omega$	3	-	17	ns
	$t_{PHL}$		2	-	12	
Propagation Delay, A or B to output Y (other input high)	$t_{PLH}$	$V_{CC} = 4.5$ to $5.5\text{V}$ , $C_L = 50\text{pF}$ , $R_L = 500\Omega$	3	-	17	ns
	$t_{PHL}$		2	-	10	

4. Not production tested in die form, characterized by chip design and tested in package.

### Switching Waveforms

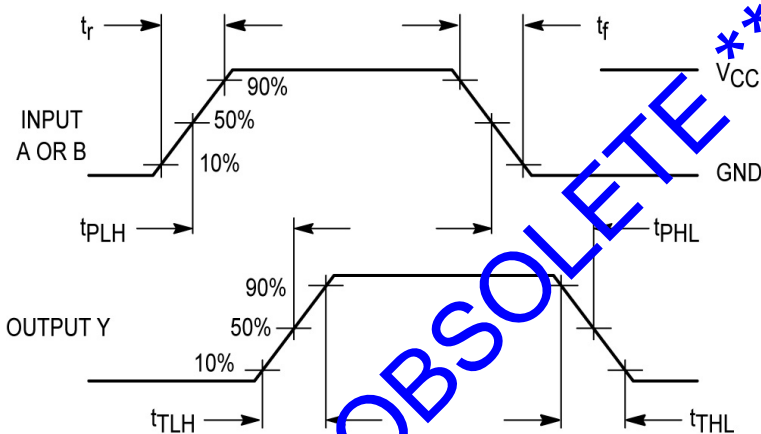


Figure 1 Propagation Delay & Timing

### Test Circuit

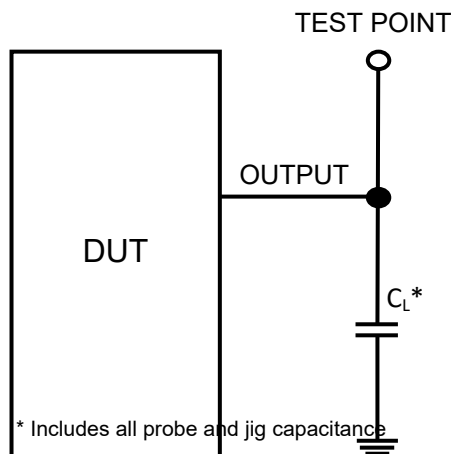


Figure 2

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