



# Advanced Low Power Schottky Logic – 74ALS00

## Quad 2-Input NAND Gates in bare die form

Rev 1.1  
23/01/24

### Description

74ALS00 provides x4 independent 2-input NAND gates performing the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$ . The device is fabricated using a 1.5µm 40V Bipolar process. Internal circuitry comprises of 3 stages and includes buffered outputs for high noise immunity and stability. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

#

### Ordering Information

The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

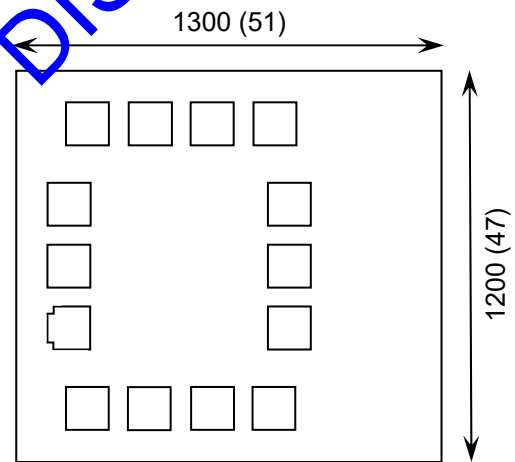
For High Reliability versions of this product please see

[54ALS00](#)

### Features:

- High speed – 3ns (Min) propagation delay
- Direct drop-in replacement for obsolete components in long term programs.

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (300 per tray capacity)
- Sawn Wafer on Tape – On request
- Unseen Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unseen)	1300 x 1200 51 x 47	µm mils
Minimum Bond Pad Size	130 x 130 5.12 x 5.12	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

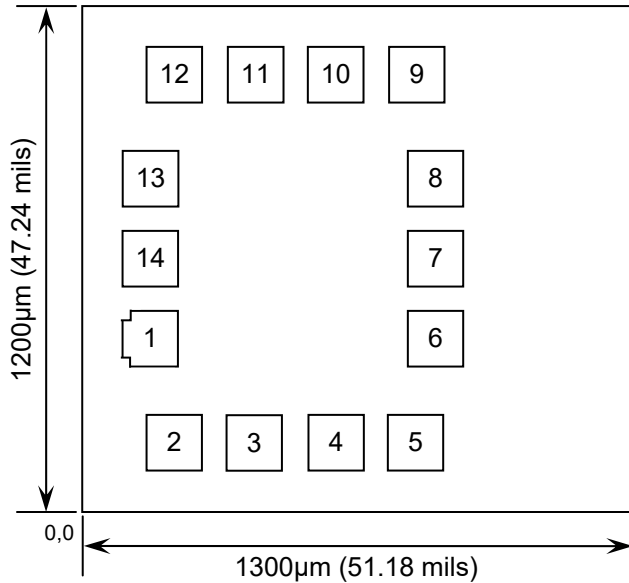




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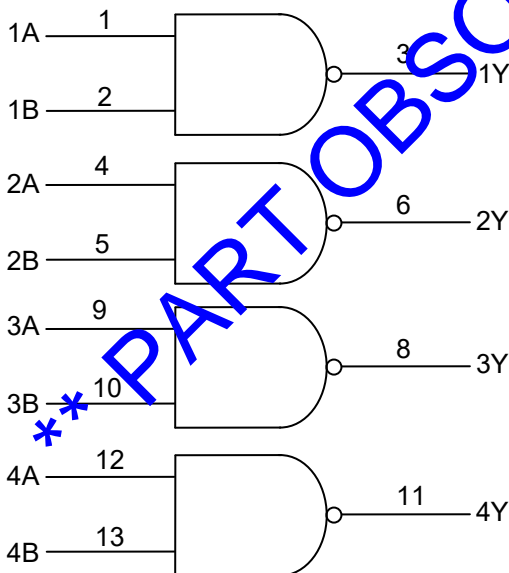
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.100	0.345
2	1B	0.155	0.100
3	1Y	0.345	0.100
4	2A	0.535	0.100
5	2B	0.725	0.100
6	2Y	0.770	0.345
7	GND	0.770	0.535
8	3Y	0.770	0.725
9	3A	0.725	0.970
10	3B	0.535	0.970
11	4Y	0.345	0.970
12	4A	0.155	0.970
13	4B	0.100	0.725
14	V <sub>CC</sub>	0.100	0.535

CONNECT CHIP BACK TO GND

## Logic Diagram



## Function Table

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High level (steady state)  
L = Low level (steady state)





## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	$V_{CC}$	7.0	V
DC Input Voltage	$V_{IN}$	7.0	V
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

## Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	$V_{CC}$	4.5	5.5	V
High-Level Input Voltage	$V_{IH}$	2	-	V
Low-Level Input Voltage	$V_{IL}$	-	0.8	V
High-Level Output Current	$I_{OH}$	-	0.4	mA
Low-Level Output Current	$I_{OL}$	-	8	mA
Operating Temperature Range	$T_J$	-40	+85	°C

## DC Electrical Characteristics<sup>2</sup> $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
Minimum High-Level Input Voltage	$V_{IH}$	-	2	-	-	V	
Maximum Low-Level Input Voltage	$V_{IL}$	-	-	-	0.8	V	
Input Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{MIN}$ $I_{IN} = -18\text{mA}$	-	-	-1.5	V	
Output Voltage High	$V_{OH}$	$V_{CC} = 4.5\text{V to } 5.5\text{V}$ , $I_{OH} = -0.4\text{mA}$	$V_{CC} - 2$	-	-	V	
Output Voltage Low	$V_{OL}$	$V_{CC} = 4.5\text{V}$	$I_{OL} = 4\text{mA}$	-	0.25	0.4	V
			$I_{OL} = 8\text{mA}$	-	0.35	0.5	
Input Current	$I_{IN}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 7\text{V}$	-	-	0.1	mA	
Input High Current	$I_{IH}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 2.7\text{V}$	-	-	20	$\mu\text{A}$	
Input Low Current	$I_{IL}$	$V_{CC} = 5.5$ , $V_{IN} = 0.4\text{V}$	-	-	-0.1	mA	
Output Current <sup>3</sup>	$I_O$	$V_{CC} = 5.5$ , $V_{OUT} = 2.25\text{V}$	-30	-	-112	mA	
Power Supply Current (Total)	$I_{CCH}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 4.5\text{V}$	-	0.5	0.85	mA	
	$I_{CCL}$	$V_{CC} = 5.5\text{V}$ , $V_{IN} = 0\text{V}$	-	1.5	3		

2. All typical values @  $V_{CC} = 5\text{V}$ ,  $T_J = 25^{\circ}\text{C}$ .

3. Output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$



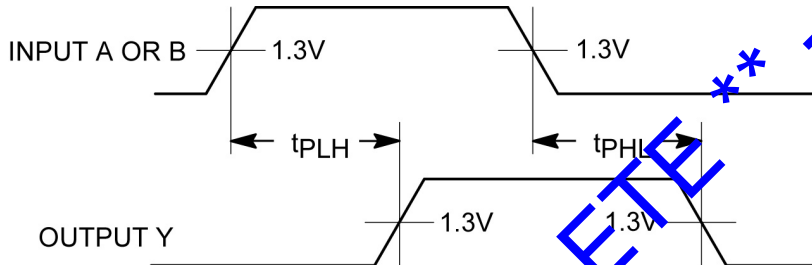


## AC Electrical Characteristics<sup>4</sup> $T_J = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ unless otherwise specified

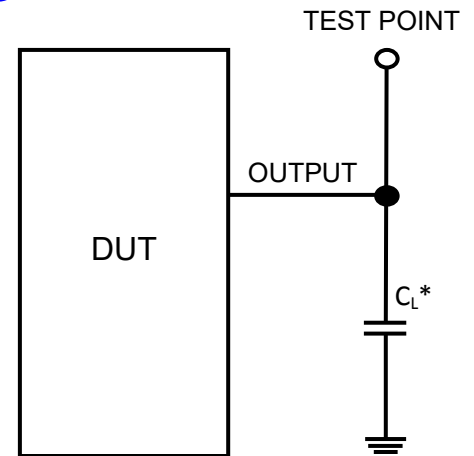
PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, A or B to output Y	$t_{PLH}$	$V_{CC} = 4.5$ to $5.5\text{V}$ , $C_L = 50\text{pF}$ , $R_L = 500\Omega$	3	-	11	ns
	$t_{PHL}$		2	-	8	

4. Not production tested in die form, characterized by chip design and tested in package.

### Switching Waveform



### Test Circuit



\* Includes all probe and jig capacitance

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