Advanced CMOS TTL Input – 74ACT574

8-bit non-inverting D-Type Flip-Flop with 3-State Outputs in bare die form

Rev 1.0
19/3/2021

Description

The 74ACT574 is fabricated using a 1.5µm 5V CMOS process combining high speed performance LSTTL performance with CMOS low power consumption. The device integrates eight D-type Flip-Flops, a buffered common Clock (CLK) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D-type inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CLK) transition. Device inputs directly accept both standard CMOS and LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- TTL / CMOS compatible Input Levels
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 4.5V to 5.5V
- Function compatible with74LS574
- Full Military Temperature Range.

Ordering Information

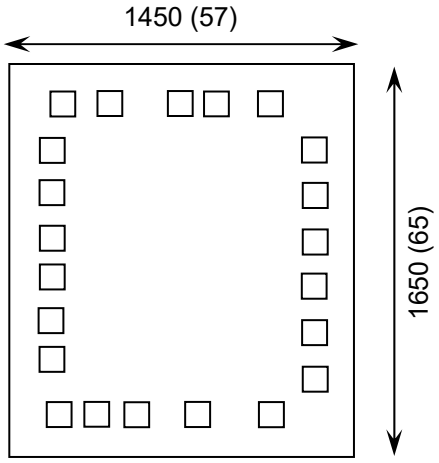
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT574

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1450 x 1650 57 x 65	µm mils
Minimum Bond Pad Size	108 x 108 4.25 x 4.25	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

Pad Layout and Functions

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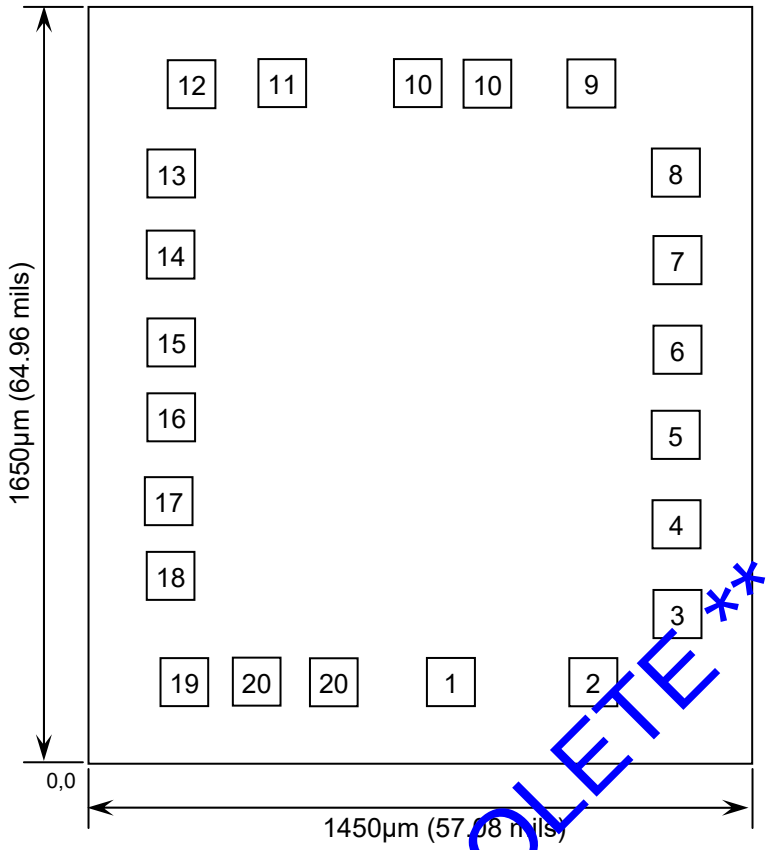
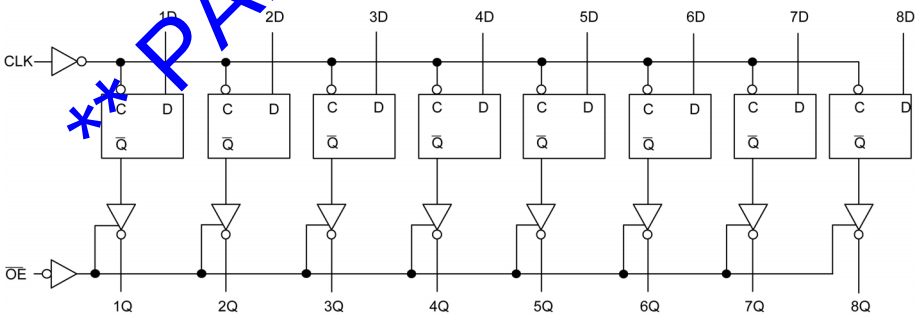


PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{OE}$	0.735	0.100
2	1D	1.050	0.100
3	2D	1.23	0.280
4	3D	1.23	0.470
5	4D	1.23	0.660
6	5D	1.23	0.860
7	6D	1.23	1.050
8	7D	1.23	1.250
9	8D	1.050	1.430
10	GND	0.810	1.430
10	GND	0.660	1.430
11	CLK	0.370	1.430
12	8Q	0.140	1.430
13	7Q	0.100	1.220
14	6Q	0.100	1.040
15	5Q	0.100	0.860
16	4Q	0.100	0.680
17	3Q	0.100	0.500
18	2Q	0.100	0.320
19	1Q	0.140	0.100
20	V_{CC}	0.320	0.100
20	V_{CC}	0.470	0.100
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 10 = GND, Pad 20 = V_{CC}

Truth Table

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L,H ↓	X	No Change
H	X	X	Z

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance
X = Don't care

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current, per pad	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-40	+85	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 0.8V to 2V)	V_{CC} = 4.5V	$\Delta t/\Delta V$	0	10	ns/V
	V_{CC} = 5.5V		0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum High-Level Output Voltage	V_{OH}	4.5V	I_{OUT} = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OH} = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	

4. -40˚C ≤ T_J ≤ +85˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	4.5V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = 24mA	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State leakage current	I_{OZ}	5.5V	V_{OUT}=V_{CC} or GND V_{IN} = V_{IL} or V_{IH}	±0.5	±2.5	±2.5	µA
Additional Maximum I_{CC} / Input	ΔI_{CCT}	5.5V	V_{IN} = V_{CC} -2.1V	1	1.5	1.5	mA
Minimum Dynamic Output Current[6]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max		75	75	mA
	I_{OHD}	5.5V	V_{OHD} = 3.85V Min		-75	-75	
Maximum Quiescent Supply Leakage Current	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	8	80	80	µA

5. All outputs loaded; thresholds on input associated with output under test. **6.** Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics[7]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency	f_{max}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	100	85	85	MHz
Propagation Delay CLK to Q (Figure 1,5)	t_{PLH}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	11	12	12	ns
	t_{PHL}			10	11	11	
Output Enable Time $\overline{OE}$ to Q (Figure 3,6)	t_{PZH}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	9.5	10	10	ns
	t_{PZL}			9.0	10	10	
Output Enable Time $\overline{OE}$ to Q (Figure 3,6)	t_{PHZ}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	10.5	11.5	11.5	ns
	t_{PLZ}			8.5	9.0	9.0	
Maximum Input Capacitance	C_{IN}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	10	10	10	pF
Power Dissipation Capacitance[7]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				40			

7. Not production tested in die form, characterized by chip design.

Timing Requirements[6]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to CLK (Figure 2,4)	t_{SU}	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	2.5	2.5	2.5	ns
Minimum Hold Time, CLK to D (Figure 2,4)	t_h	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	1.0	1.0	1.0	ns
Minimum Pulse Width, CLK (Figure 2,4)	t_w	5V ±0.5	C_L = 50pF, Input t_f =t_r= 3ns	3.0	4.0	4.0	ns

Switching Waveforms

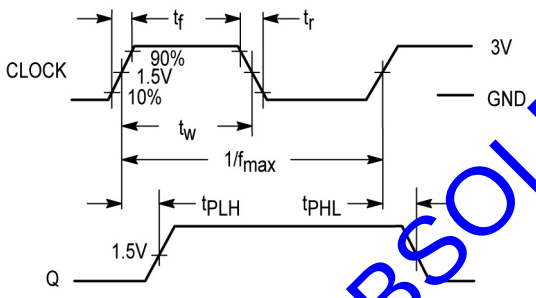


Figure 1 – Propagation Delay & Output Transition Time

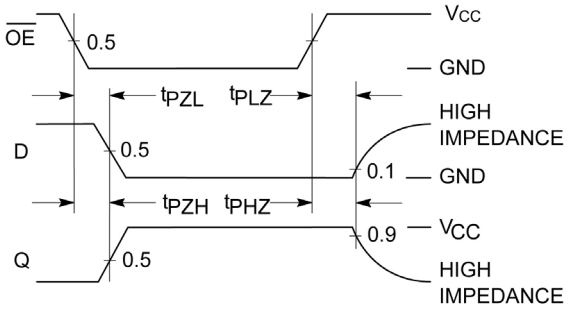


Figure 3 – Propagation Delay - Output Enable to Q

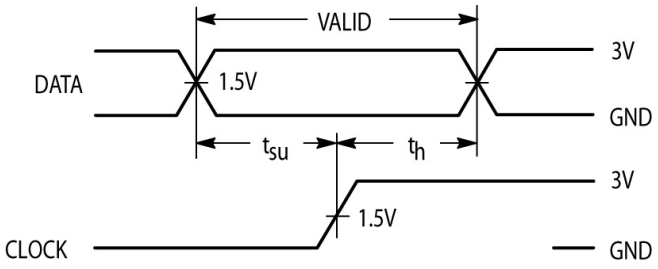
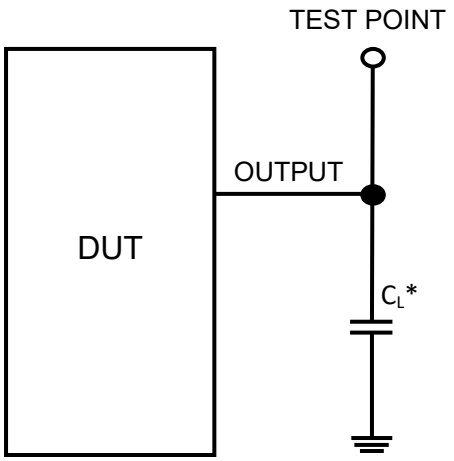


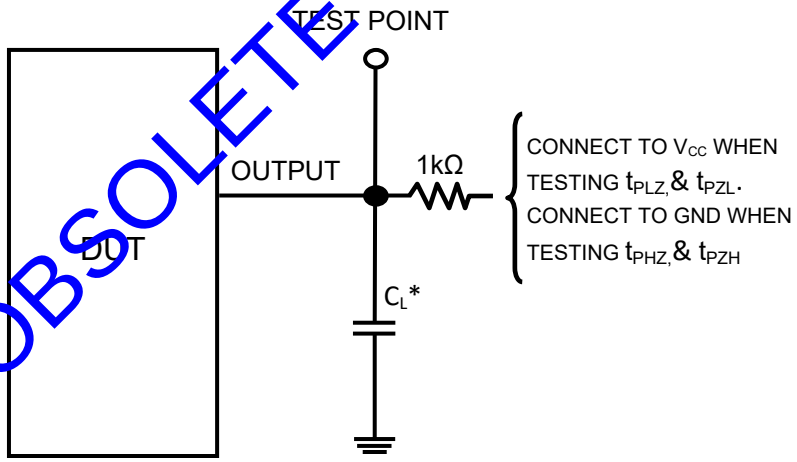
Figure 4 – Timing Requirements

Test Circuits



* Includes all probe and jig capacitance

Figure 5



* Includes all probe and jig capacitance

Figure 6