Advanced CMOS TTL Input – 74ACT38

Quad 2-input NAND buffer (open drain) in bare die form

Rev 1.0
18/01/21

Description

74ACT38 provides x4 independent 2-input NAND gates performing the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$. The device is fabricated using an advanced 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power consumption. The provision of open-drain outputs enables implementation of active-low wired-OR or active-high wired-AND functionality. Device inputs directly accept both standard CMOS and LSTTL outputs. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Open-drain output for wired-OR/wired-AND function
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 74LS38, 74F38
- Lower power alternative to bipolar logic.

Ordering Information

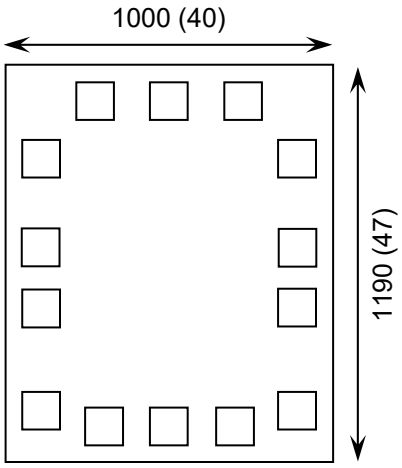
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

54ACT38

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1000 x 1190 40 x 47	µm mils
Minimum Bond Pad Size	100 x 100 4 x 4	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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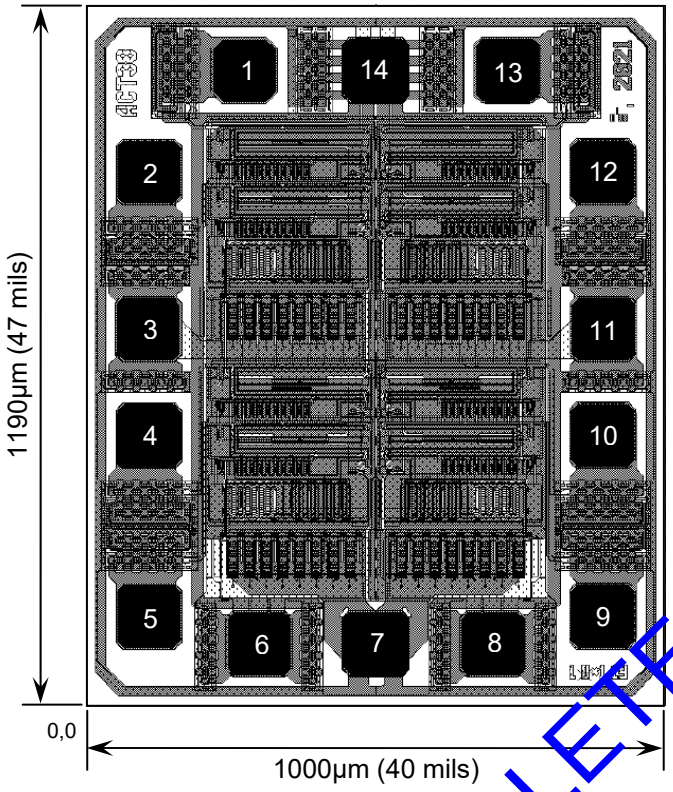
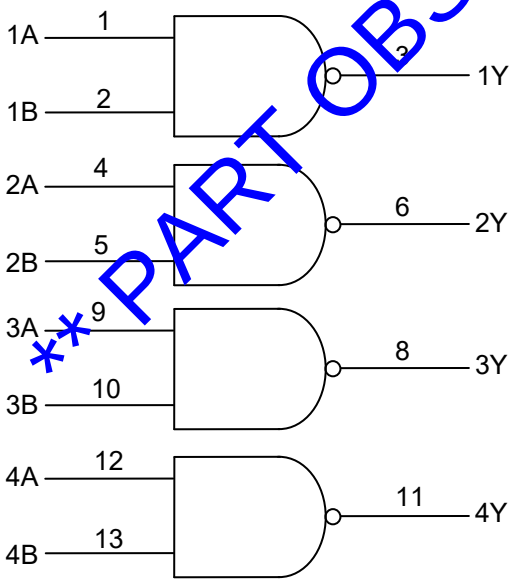
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	1A	0.250	0.980
2	1B	0.100	0.820
3	1Y	0.100	0.580
4	2A	0.100	0.420
5	2B	0.100	0.140
6	2Y	0.270	0.100
7	GND	0.450	0.100
8	3Y	0.670	0.100
9	3A	0.790	0.140
10	3B	0.790	0.420
11	4Y	0.790	0.590
12	4A	0.790	0.820
13	4B	0.650	0.980
14	V_{CC}	0.450	0.980
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

H = High level (steady state)
L = Low level (steady state)
Z = High Impedance state

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input or Output Voltage (Referenced to GND)	V_{IN}, V_{OUT}	-0.5 to V_{CC}+0.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±20	mA
Output Current (per Pad)	I_{OUT}	±50	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	500	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic SSOP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages Referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
DC Supply Voltage		V_{CC}	4.5	5.5	V
DC Input or Output Voltage		V_{IN} ,V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Output current - High		I_{OH}	-	-24	mA
Output current - Low		I_{OL}	-	24	mA
Input Rise or Fall rate (V_{IN} from 0.8V to 2V)	V_{CC} = 4.5V	$\Delta t/\Delta V$	0	10	ns/V
	V_{CC} = 5.5V		0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS 25°C	LIMITS 85°C	LIMITS FULL RANGE[4]	UNITS
Minimum High-Level Input Voltage	V_{IH}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	V_{IL}	4.5V	V_{OUT} = 0.1V or V_{CC} -0.1V	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum Low-Level Output Voltage	V_{OL}	4.5V	I_{OUT} = 50µA	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = 24mA	0.36	0.44	0.44	V
		5.5V		0.36	0.44	0.44	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5,6] I_{OL} = 50mA	1.65	1.65	1.65	V
		5.5V		1.65	1.65	1.65	

4. -40˚C ≤ T_J ≤ +85˚C **5.** All outputs loaded; thresholds on input associated with output under test. **6.** Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 85°C

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Output Voltage	V_{OH}	4.5V	I_{OUT} = -50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5] I_{OL} = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	
		4.5V	V_{IN} = V_{IL} or V_{IH}[5,6] I_{OL} = -50mA	-	-	-	V
		5.5V		-	-	-	
Maximum Input Leakage Current	I_{IN}	5.5V	V_{IN} = V_{CC} or GND	±0.1	±1.0	±1.0	µA
Maximum 3-State leakage current	I_{OZ}	5.5	V_{OUT}=V_{CC} or GND, V_{IN} = V_{IL} or V_{IH}	±0.5	±2.5	±2.5	µA
Additional Maximum I_{CC} / Input	ΔI_{CCT}	5.5V	V_{IN} = V_{CC} -2.1V	0.6	1.5	1.5	mA
Minimum Dynamic Output Current[7]	I_{OLD}	5.5V	V_{OLD} = 1.65V Max	-	75	75	mA
	I_{OHD}	5.5V	V_{OHD} = 3.86V Min	-	-75	-75	
Maximum Quiescent Supply Leakage Current	I_{CC}	5.5V	V_{IN} = V_{CC} or GND I_{OUT} = 0µA	4	40	40	µA

7. Maximum test duration 2ms, one output loaded at a time.

AC Electrical Characteristics[8]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, A or B to Y	t_{PLH}	5V ±10%	GND = 0V, C_L = 50pF, R_L = 500Ω, t_r = t_f = ≤ 2.5ns	6	7	7	ns
	t_{PHL}			6	7	7	
Maximum Propagation Delay, OFF-state to Low	t_{PZL}	5V ±10%	GND = 0V, C_L = 50pF, R_L = 500Ω, t_r = t_f = ≤ 2.5ns, (Figure1)	5.1	6	6	ns
Maximum Propagation Delay, Low to OFF-state	t_{PLZ}			5.0	5.3	5.3	
Maximum Input Capacitance	C_{IN}	5V ±10%	V_{IN} = V_{CC} or GND	8	8	8	pF
Power Dissipation Capacitance[9]	C_{PD}	-	T_J = 25°C, V_{CC} =5.0V	TYPICAL			pF
				40			

8. Not production tested in die form, characterized by chip design.
9. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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Switching Waveforms

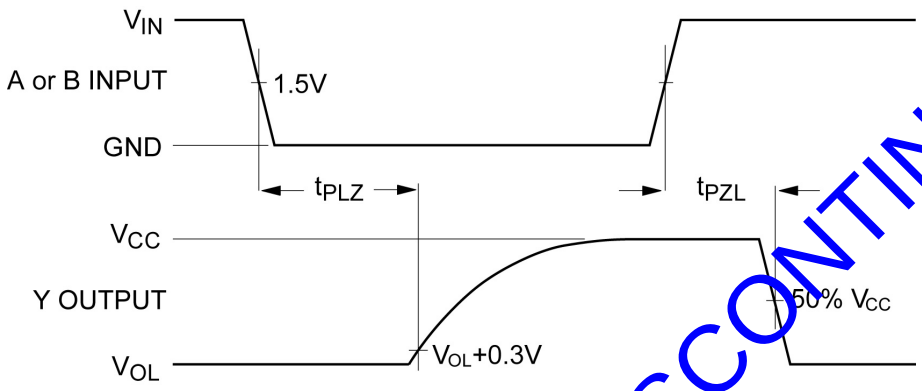
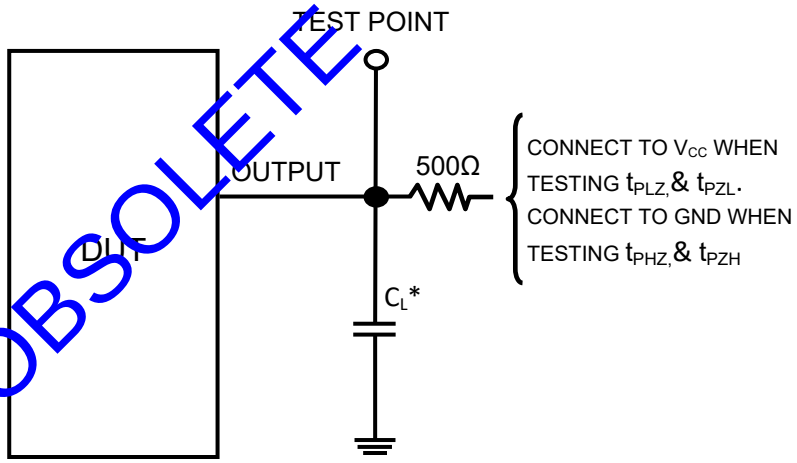


Figure 1 – Propagation Delay, Input A or B to Output Y

Test Circuit



* Includes all probe and jig capacitance