



# Advanced CMOS Logic – 74ACT08

## Quad 2-Input AND Gate in bare die form

Rev 1.0  
06/02/20

### Description

The 74ACT08 quad 2-input AND gate is fabricated using a 1.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device consists of four independent 2-input AND gates with standard push-pull outputs and performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A + B}$ . Device inputs are compatible with standard CMOS outputs and also directly compatible with LSTTL outputs. All inputs are protected against ESD and excess voltage transients.

### Features:

- Inputs directly accept TTL
- Outputs directly interface CMOS, NMOS and TTL
- Outputs Source/Sink 24 mA
- Low Input Current: 1µA
- Functionally compatible with bipolar 74LS08
- Lower power alternative to bipolar logic.

### Ordering Information

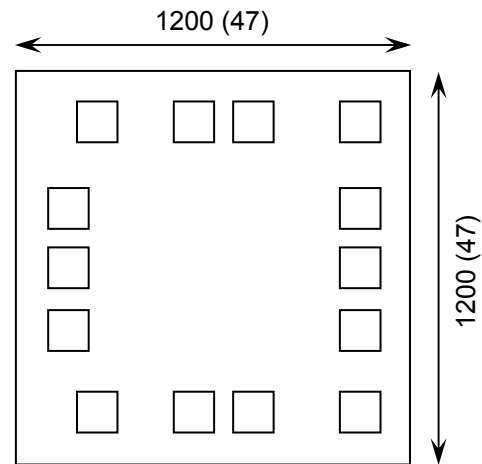
The following part suffixes apply:

- No suffix - MIL-STD-883 /2010B Visual Inspection

For High Reliability versions of this product please see

[54ACT08](#)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- ~~\*\*\*~~ Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1200 x 1200 47 x 47	µm mils
Minimum Bond Pad Size	120 x 120 4.72 x 4.72	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

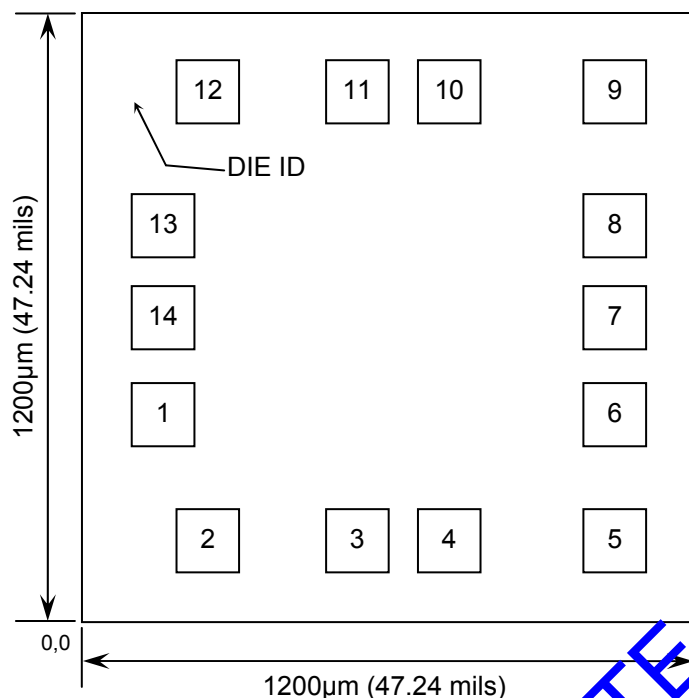




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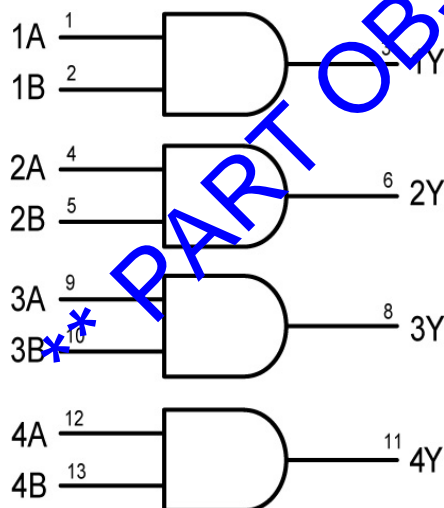
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	150	350
2	1B	150	100
3	1Y	480	100
4	2A	660	100
5	2B	990	100
6	2Y	990	350
7	GND	990	540
8	3Y	990	720
9	3A	990	980
10	3B	660	980
11	4Y	480	980
12	4A	150	980
13	4B	100	720
14	V <sub>CC</sub>	100	540

CONNECT CHIP BACK TO V<sub>CC</sub> OR FLOAT

## Logic Diagram



## Function Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High level (steady state)  
L = Low level (steady state)





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	$I_{IN}$	±20	mA
DC Output Current, per pad	$I_{OUT}$	±50	mA
DC Supply Current, $V_{CC}$ or GND, per pad	$I_{CC}$	±50	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages Referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
DC Supply Voltage	$V_{CC}$	4.5	5.5	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-40	+85	°C	
Output current - High	$I_{OH}$	-	-24	mA	
Output current - Low	$I_{OL}$	-	24	mA	
Input Rise or Fall rate ( $V_{IN}$ from 0.8V to 2V)	$\Delta V/\Delta V$	$V_{CC} = 4.5V$	0	10	ns/V
		$V_{CC} = 5.5V$	0	8	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	$V_{IH}$	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	2	2	2	V
		5.5V		2	2	2	
Maximum Low-Level Input Voltage	$V_{IL}$	4.5V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	0.8	0.8	0.8	V
		5.5V		0.8	0.8	0.8	
Minimum Low-Level Output Voltage	$V_{OL}$	4.5V	$I_{OUT} = 50\mu A$	0.1	0.1	0.1	V
		5.5V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^5$	0.36	0.44	0.44	V
		5.5V	$I_{OL} = 24mA$	0.36	0.44	0.44	
		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IH}^{5,6}$	-	-	1.65	V
		5.5V	$I_{OL} = 50mA$	-	-	1.65	

4.  $-40^\circ C \leq T_J \leq +85^\circ C$  5. All outputs loaded; thresholds on input associated with output under test. 6. Test time 1sec max, measurement made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 75Ω transmission-line drive capability at 125°C





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## DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Output Voltage	V <sub>OH</sub>	4.5V	I <sub>OUT</sub> = 50µA	4.4	4.4	4.4	V
		5.5V		5.4	5.4	5.4	
		4.5V	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> <sup>5</sup> I <sub>OH</sub> = -24mA	3.86	3.76	3.76	V
		5.5V		4.86	4.76	4.76	
Maximum Input Leakage Current	I <sub>IN</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	µA
Additional Maximum I <sub>CC</sub> / Input	ΔI <sub>CC</sub> T	5.5V	V <sub>IN</sub> = V <sub>CC</sub> - 2.1V	0.6	1.5	1.5	mA
Minimum Dynamic Output Current <sup>7</sup>	I <sub>OLD</sub>	5.5V	V <sub>OLD</sub> = 1.65V Max	-	75	75	mA
	I <sub>OHD</sub>	5.5V	V <sub>OHD</sub> = 3.85V Min	-	-75	-75	
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	5.5V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0µA	4	40	40	µA

7. Maximum test duration 2ms, one output loaded at a time.

## AC Electrical Characteristics<sup>8</sup> V<sub>CC</sub> = 5.0V ± 0.5V

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay Input A or B to Output Y (Figure 1)	t <sub>PLH</sub>	5.0V	C <sub>L</sub> = 50pF, Input tr = tf = 3.0ns	9	10	10	ns
	t <sub>PHL</sub>	5.0V		9	10	10	
Maximum Input Capacitance	C <sub>IN</sub>	5.0V	T <sub>J</sub> = 25°C	TYPICAL			pF
				4.5			
Power Dissipation Capacitance	C <sub>PD</sub>	5.0V	T <sub>J</sub> = 25°C, C <sub>L</sub> = 50pF	20			pF

8. Not production tested in die form, characterized by chip design and tested in package.





## Switching Waveform

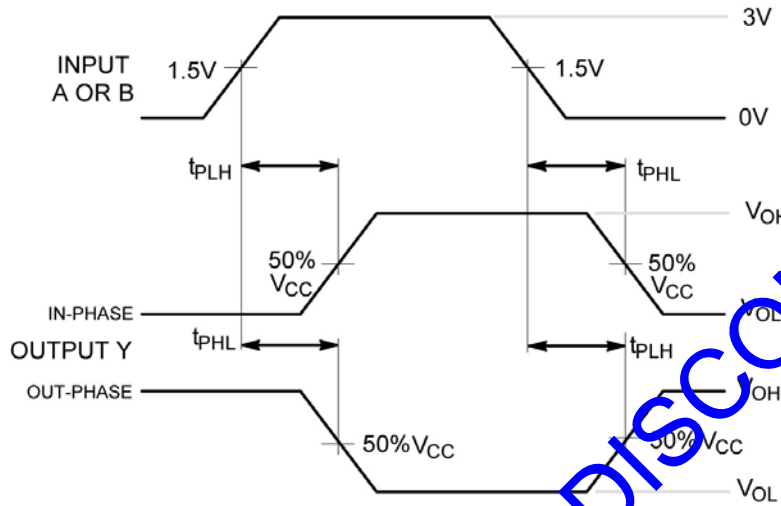
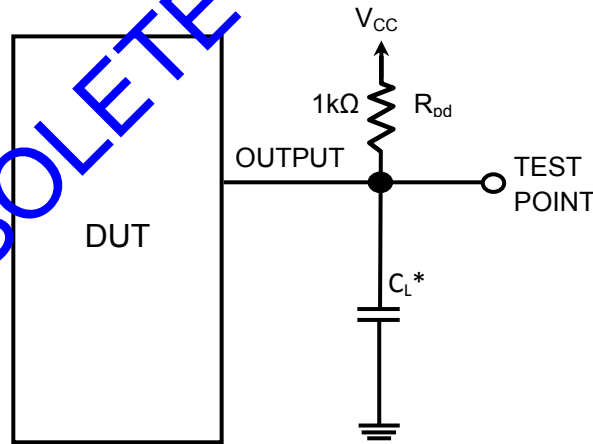


Figure 1 – Propagation Delay

## Test Circuit



\* Includes all probe and jig capacitance

Figure 2

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