Low Power Schottky Logic – 54LS164

8-Bit Serial-Input / Parallel-Output Shift Register in bare die form

Rev 1.0
24/11/17

Description

The 54LS164 is fabricated on a 2µm 40V Bipolar process. The device consists of x2 serial data inputs, A and B, provided so that one input can be used as a data enable. Data is entered on each rising edge of the clock. A LOW on the master reset input ($\overline{CLR}$) clears the register, forcing all outputs LOW, independent of other inputs. All inputs are equipped with Schottky clamp diodes to limit termination effects & achieve high speed. These input circuits also protect against static discharge & transient excess voltage.

Features:

- Aysnchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Direct drop-in replacement for obsolete components in long term programs.
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

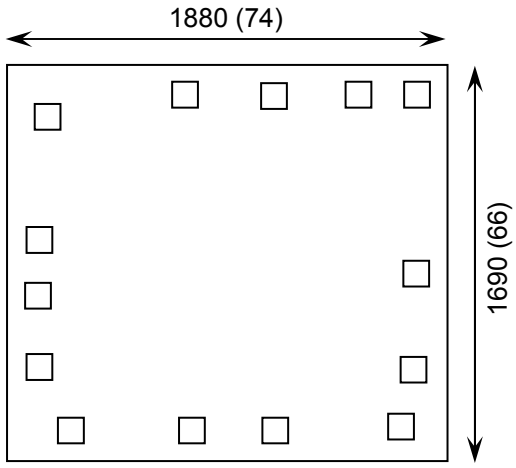
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1880 x 1690 74 x 67	µm mils
Minimum Bond Pad Size	110 x 110 4.33 x 4.33	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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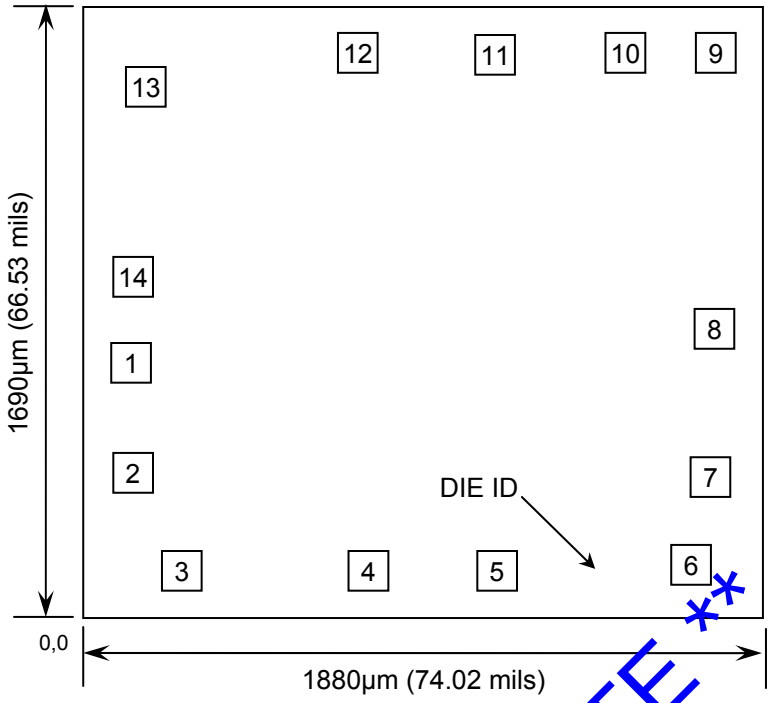
Pad Layout and Functions



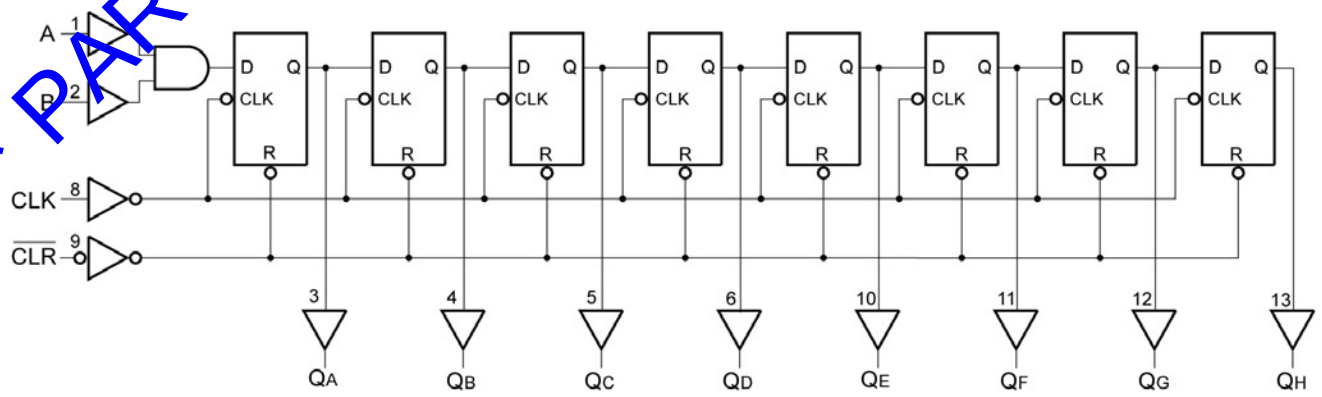
PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	A	0.075	0.647
2	B	0.077	0.342
3	Q_A	0.203	0.075
4	Q_B	0.725	0.075
5	Q_C	1.091	0.075
6	Q_D	1.625	0.083
7	GND	1.691	0.331
8	CLK	1.693	0.745
9	$\overline{CLR}$	1.691	1.504
10	Q_E	1.449	1.505
11	Q_F	1.091	1.503
12	Q_G	0.697	1.505
13	Q_H	0.085	1.412
14	V_{CC}	0.077	0.885
CONNECT CHIP BACK TO GND OR FLOAT			

Function Table

INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B	… Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{Gn}

Logic Diagram

D = Data Input
Q_{An} - Q_{Gn} = Data shift from preceding register on rising edge clock input



Rev 1.0
24/11/17

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{CC}	7.0	V
DC Input Voltage	V_{IN}	7.0	V
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{CC}	4.5	5.5	V
High-Level Input Voltage	V_{IH}	2		V
Low-Level Input Voltage	V_{IL}	-	0.7	V
High-Level Output Current	I_{OH}	-	-0.4	mA
Low-Level Output Current	I_{OL}	-	4	mA
Clock Frequency	f_{clock}	0	25	MHz
Pulse Width – Clock or Clear	t_w	20	-	ns
Setup time – A or B to Clock	t_{su}	15	-	ns
Recovery Time	t_{rec}	5	-	ns
Operating Temperature Range	T_J	-55	+125	°C

DC Electrical Characteristics[2] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Minimum High-Level Input Voltage	V_{IH}	-		2	-	-	V
Maximum Low-Level Input Voltage	V_{IL}	-		-	-	0.7	V
Input Clamp Diode Voltage	V_{IK}	V_{CC} = MIN I_{IN} = -18mA		-	-	-1.5	V
Output Voltage High	V_{OH}	V_{CC} = MIN, I_{OH} = -0.4mA V_{IH} = 2V, V_{IL} = MAX		2.5	3.5	-	V
Output Voltage Low	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = MAX	I_{OL} = 4mA	-	0.25	0.4	V

2. All typical values @ V_{CC} = 5V, T_J = 25°C.

Rev 1.0
24/11/17

DC Electrical Characteristics continued [2] T_J = -55°C to 125°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input High Current	I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V	-	-	20	µA
		V_{CC} = MAX, V_{IN} = 7.0V	-	-	0.1	mA
Input Low Current	I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V	-	-	-0.4	mA
Short Circuit Current[3]	I_{OS}	V_{CC} = MAX	-20	-	-100	mA
Power Supply Current (Total)	I_{CC}	V_{CC} = MAX	-	16	27	mA

3. Not more than one output should be shorted at a time, nor for more than 1 second.

AC Electrical Characteristics[4] T_J = 25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Propagation Delay, Clock to Q	t_{PLH}	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	-	-	27	ns
Propagation Delay, Clock to Q	t_{PHL}	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	-	-	32	ns
Propagation Delay, Reset to Q	t_{PHL}	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	-	-	36	ns

Timing Requirements[4] T_J = 25°C unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Setup Time, A or B to CLK	t_{su}	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	15	-	-	ns
Hold Time, CLK to A or B	t_h	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	5	-	-	ns
Pulse Width, Clock or Reset	t_w	V_{CC} = 5V, C_L = 15pF, R_L =2kOhm, t_r = 15ns, t_r = 6ns	20	-	-	ns

4. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveforms

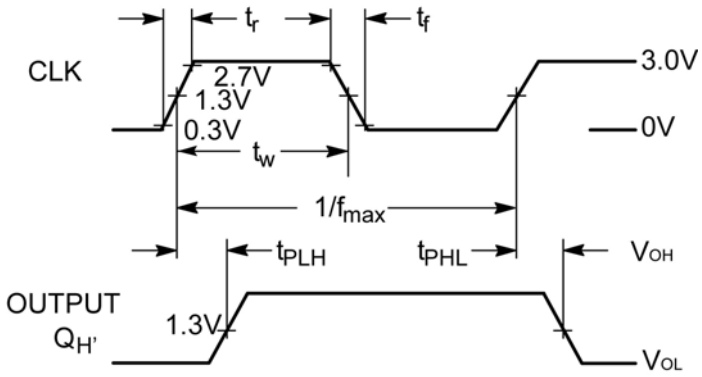


Figure 1 – Clock Propagation Delay & Output Timing

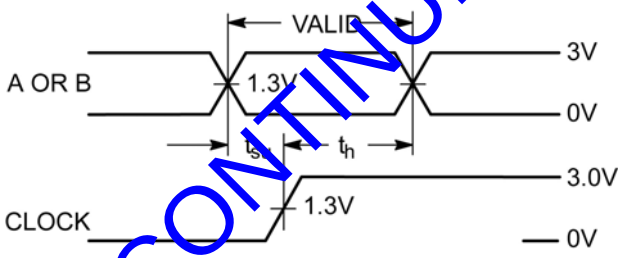


Figure 2 – Data Transition Timing, Serial Input & Clock

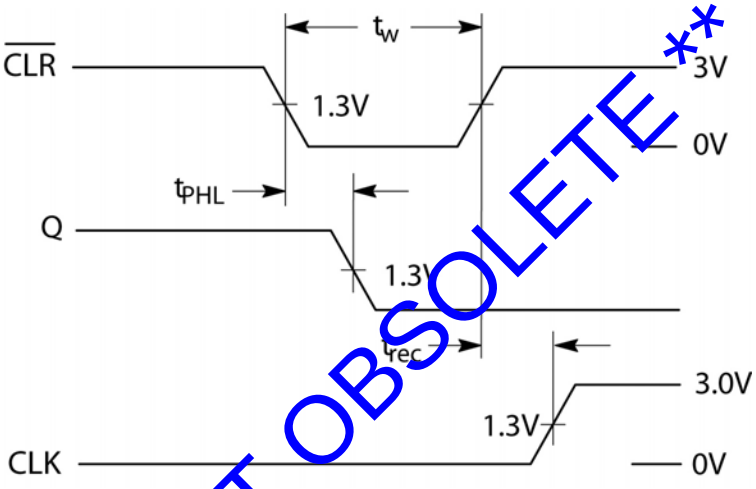
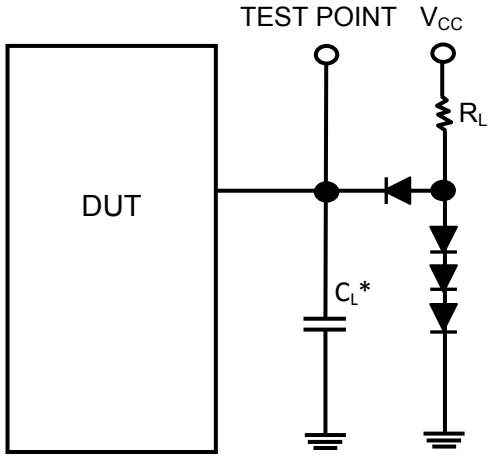


Figure 3 – Reset to Output Propagation Delay & Timing



- Includes all probe and jig capacitance
  All diodes are 1N914

Figure 4 – Test Setup