High Speed CMOS Logic – 54HC74

Dual D-Type Flip-Flop Logic IC with Set and Reset in bare die form

Rev 1.0
21/11/17

Description

The 54HC74 is fabricated using a 2.5µm 5V CMOS process and consists of two identical, independent data type flip-flops. Each flip-flop has separate data, set, reset, clock inputs and Q,$\overline{Q}$ outputs. The device can be used in Shift Register applications and also Counter or Toggle applications by connecting Q output to the data input. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is clock independent and accomplished by a high level on the respective Set or Reset line.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Low Input Current: 1µA
- Asynchronous Set-Reset Capability
- ±4mA Output Drive at 5V
- Operating Voltage Range: 2.0 to 6.0 V
- Direct drop in replacement for obsolete components in long term programs.

Ordering Information

The following part suffixes apply:

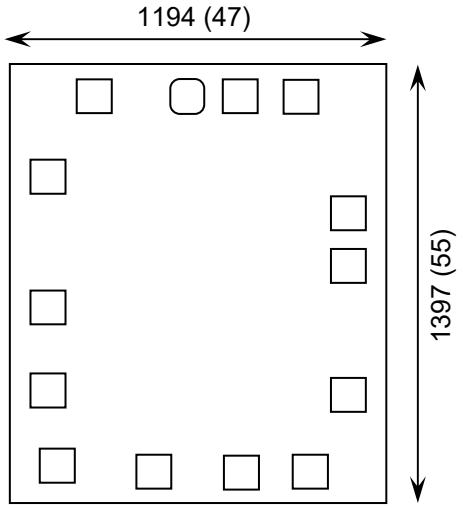
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1194 x 1397 47 x 55	µm mils
Minimum Bond Pad Size	100 x 100 3.94 x 3.94	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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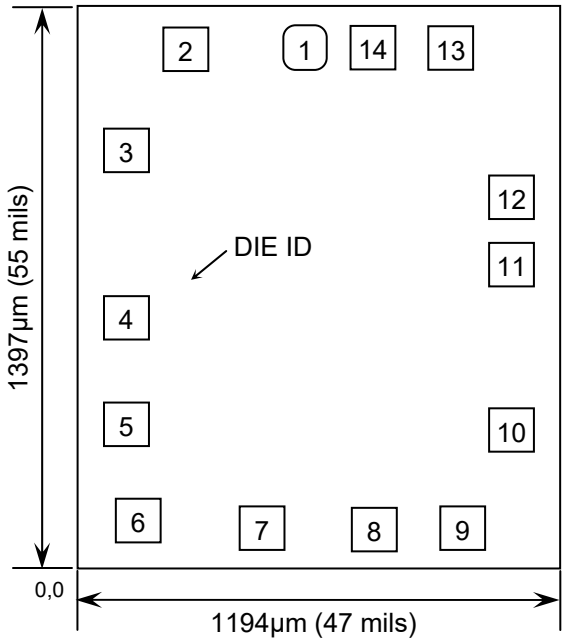
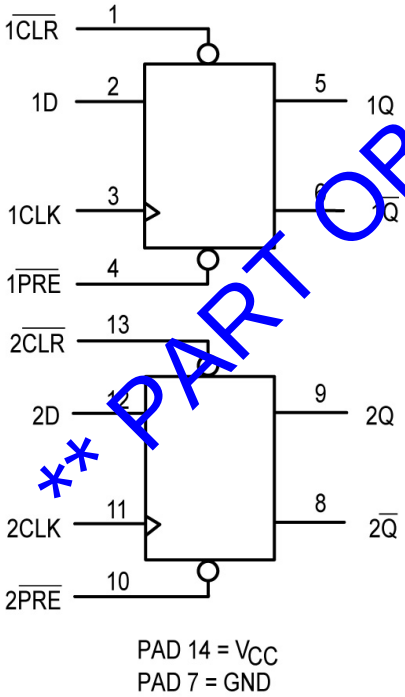
Pad Layout and Functions



PAD	FUNCTION
1	1$\overline{CLR}$
2	1D
3	1CLK
4	1$\overline{PRESET}$
5	1$\overline{Q}$
6	1Q
7	GND
8	2$\overline{Q}$
9	2Q
10	2$\overline{PRESET}$
11	2CLK
12	2D
13	2 $\overline{CLR}$
14	V_{CC}
CONNECT CHIP BACK TO V_{CC} OR FLOAT	

Logic Diagram



PAD 14 = V_{CC}
PAD 7 = GND

Truth Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

* BOTH OUTPUTS WILL REMAIN HIGH AS LONG AS SET AND RESET ARE LOW, OUTPUT STATES ARE UNPREDICTABLE IF SET AND RESET GO HIGH SIMULTANEOUSLY.

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input or Output Voltage (Referenced to GND)	V_{IN}, V_{OUT}	-1.5 to V_{CC}+1.5	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Input Current (per Pad)	I_{IN}	±20	mA
Output Current (per Pad)	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER		SYMBOL	MIN	MAX	UNITS
Supply Voltage		V_{CC}	2.0	6.0	V
DC Input Voltage, Output Voltage		V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature Range		T_J	-55	+125	°C
Input Rise / Fall Time	V_{CC}=2.5V	t_r, t_f	0	1000	ns
	V_{CC}=4.5V		0	500	
	V_{CC}=6.0V		0	400	

3. This device contains protection circuitry against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of voltage higher than max rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must be tied to an appropriate logic voltage level (e.g., GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0	V_{OUT} = 0.1V or V_{CC} -0.1V | I_{OUT} | ≤ 20µA	1.5	1.5	1.5	V
		4.5		3.15	3.15	3.15	
		6.0		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0	V_{OUT} = 0.1V or V_{CC} -0.1V | I_{OUT} | ≤ 20µA	0.5	0.5	0.5	V
		4.5		1.35	1.35	1.35	
		6.0		1.8	1.8	1.8	
Minimum High-Level Output Voltage	V_{OH}	2.0	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 20µA	1.9	1.9	1.9	V
		4.5		4.4	4.4	4.4	
		6.0		5.9	5.9	5.9	
		4.5	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 4.0mA	3.98	3.84	3.7	V
		6.0	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 5.2mA	5.48	5.34	5.2	V

DC Electrical Characteristics Continued (Voltages referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5		0.1	0.1	0.1	
		6.0		0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	0.26	0.33	0.4	V
		6.0	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 5.2mA$	0.26	0.33	0.4	
Maximum Input Leakage Current	I_{IN}	6.0	V_{IN} = GND or V_{CC}	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Current	I_{CC}	6.0	V_{IN} = GND or V_{DD} $I_{OUT} = 0\mu A$	2.0	20	80	µA

4. -55˚C ≤ T_J ≤ +125˚C

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Clock Frequency	f_{max}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	6.0	4.8	4.0	MHz
		4.5		30	24	20	
		6.0		35	28	24	
Propagation Delay, CLK to Q or $\overline{Q}$ (Figure 1)	t_{PLH}, t_{PHL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	100	125	50	ns
		4.5		20	25	30	
		6.0		17	21	26	
Propagation Delay, $\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$ (Figure 2)	t_{PLH}, t_{PHL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	105	130	160	ns
		4.5		21	26	32	
		6.0		18	22	27	
Output Transition Time, Any Output (Figure 1)	t_{TLH}, t_{THL}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	75	95	110	ns
		4.5		15	19	22	
		6.0		13	16	19	
Input Capacitance	C_{IN}	-	C_L = 50pF, $t_r = t_f$ = 6ns	10	10	10	pF
Power Dissipation Capacitance (Per Flip-Flop)	C_{PD}	-	T_J = 25°C, V_{CC} = 5.0V	TYPICAL			pF
				39			

5. Not production tested in die form, characterized by chip design and tested in package.

Timing Requirements[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum Setup Time, D to CLK (Figure 3)	t_{su}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	80	100	120	ns
		4.5		16	20	24	
		6.0		14	17	20	
Minimum Hold Time, CLK to D (Figure 3)	t_h	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	3.0	3.0	3.0	ns
		4.5		3.0	3.0	3.0	
		6.0		3.0	3.0	3.0	
Minimum Recovery Time, $\overline{PRE}$ or $\overline{CLR}$ Inactive to CLK (Figure 2)	t_{rec}	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	8.0	8.0	8.0	ns
		4.5		8.0	8.0	8.0	
		6.0		8.0	8.0	8.0	
Minimum Pulse Width, CLK (Figure 1)	t_w	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	60	75	90	ns
		4.5		12	15	18	
		6.0		10	13	15	
Minimum Pulse Width, $\overline{PRE}$ or $\overline{CLR}$ (Figure 2)	t_w	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	60	75	90	ns
		4.5		12	15	18	
		6.0		10	13	15	
Maximum Input Rise and Fall Times (Figure 1)	t_r, t_f	2.0	C_L = 50pF, $t_r = t_f$ = 6ns	1000	1000	1000	ns
		4.5		500	500	500	
		6.0		400	400	400	

5. Not production tested in die form, characterized by chip design and tested in package.

Switching Waveforms

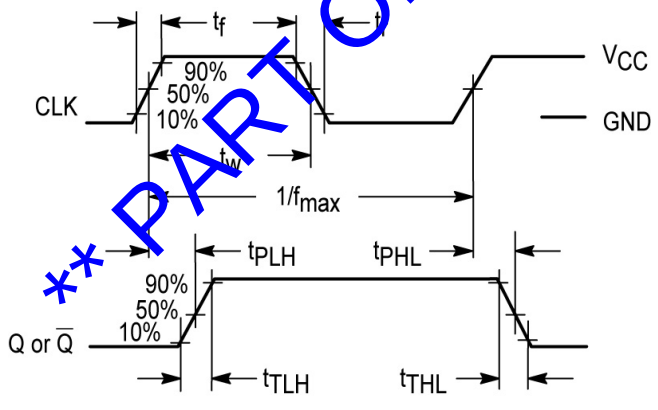

Figure 1 – Data, Clock and Output

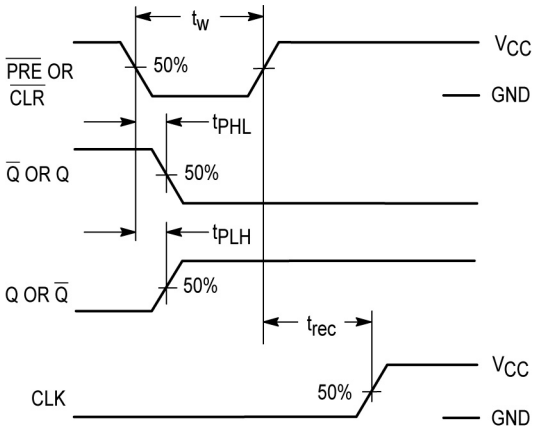

Figure 2 – Set, Reset, Clock and Output

Switching Waveforms continued

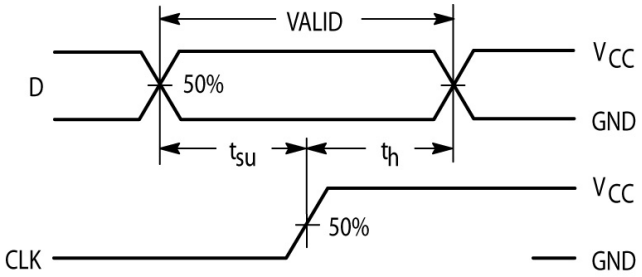

Figure 3 – Clock to Data