



# High Speed CMOS Logic – 54HC125

## Quad 3-State Non-inverting Buffers in bare die form

Rev 1.0  
22/04/19

### Description

The 54HC125 4-bit non-inverting buffer/line driver is fabricated on a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device contains four independent buffer gates with 3-state outputs each controlled by the output enable input. A HIGH at the output enable input causes the outputs to assume a HIGH impedance OFF-state. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

### Features:

- Output Drive Capability: 15 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 54LS125
- High Noise Immunity CMOS process
- Full Military Temperature Range.

### Ordering Information

The following part suffixes apply:

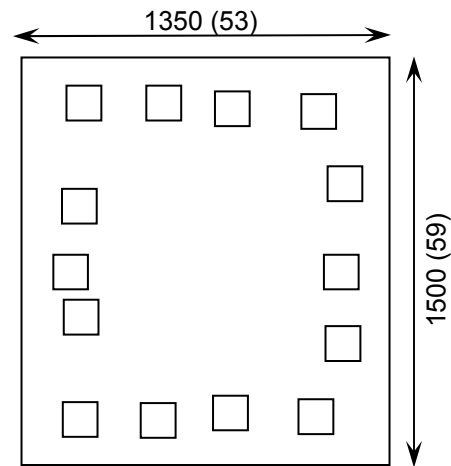
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "H" - MIL-STD-883 /2010B Visual Inspection + MIL-PRF-38534 Class H LAT
- "K" - MIL-STD-883 /2010A Visual Inspection (Space) + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

[www.siliconsupplies.com/quality/bare-die-lot-qualification](http://www.siliconsupplies.com/quality/bare-die-lot-qualification)

### Die Dimensions in µm (mils)



### Supply Formats:

- Default – Die in Waffle Pack (100 per tray capacity)
- ~~\*\*\*~~ Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <=> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

### Mechanical Specification

Die Size (Unsawn)	1350 x 1500 53 x 59	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

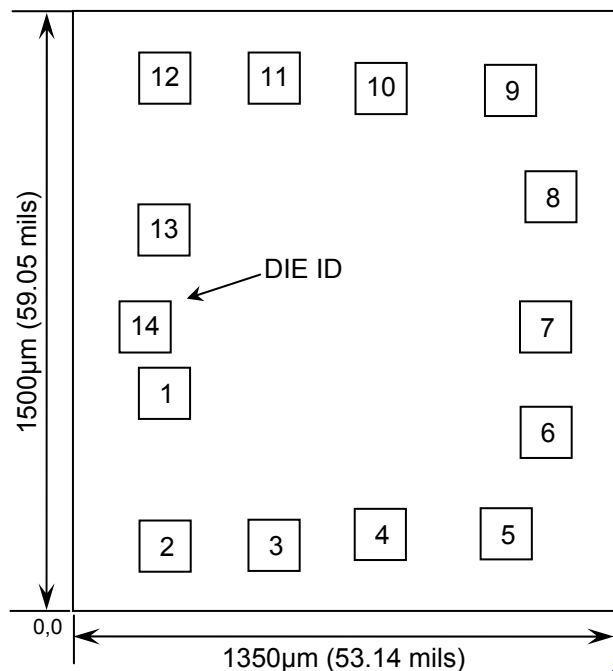




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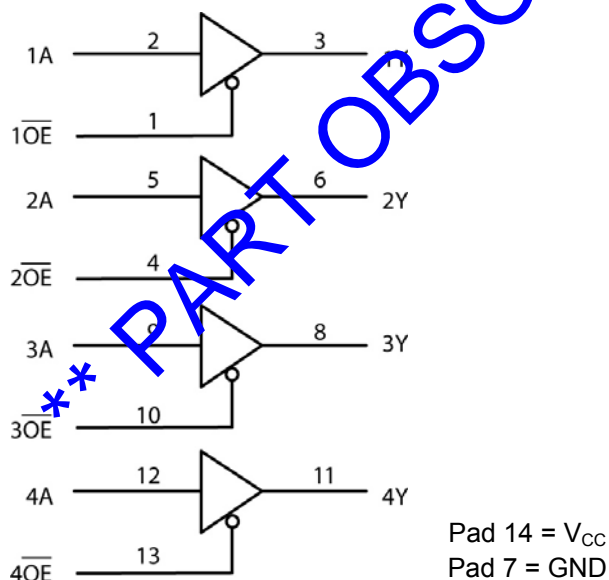
## Pad Layout and Functions



PAD	FUNCTION	COORDINATES (mm)	
		X	Y
1	$\overline{1OE}$	0.169	0.49
2	1A	0.169	0.122
3	1Y	0.464	0.122
4	$\overline{2OE}$	0.722	0.147
5	2A	1.031	0.147
6	2Y	1.124	0.408
7	GND	1.124	0.669
8	3Y	1.124	0.986
9	3A	1.051	1.247
10	$\overline{3OE}$	0.722	1.247
11	4Y	0.464	1.272
12	4A	0.169	1.272
13	$\overline{4OE}$	0.169	0.903
14	$V_{CC}$	0.128	0.66

CONNECT CHIP BACK TO  $V_{CC}$  OR FLOAT

## Logic Diagram



## Truth Table

INPUTS		OUTPUT
A	$\overline{OE}$	Y
H	L	H
L	L	L
X	H	Z

H = High level (steady state)  
L = Low level (steady state)  
X = don't care





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## Absolute Maximum Ratings<sup>1</sup>

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	$V_{CC}$	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC Output Voltage (Referenced to GND)	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC Input Current	$I_{IN}$	$\pm 20$	mA
DC Output Current, per pad	$I_{OUT}$	$\pm 35$	mA
DC Supply Current, $V_{CC}$ or GND	$I_{CC}$	$\pm 75$	mA
Power Dissipation in Still Air <sup>2</sup>	$P_D$	750	mW
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}C$

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

## Recommended Operating Conditions<sup>3</sup> (Voltages referenced to GND)

PARAMETER	SYMBOL	MIN	MAX	UNITS	
Supply Voltage	$V_{CC}$	2	6	V	
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	$V_{CC}$	V	
Operating Temperature Range	$T_J$	-55	+125	$^{\circ}C$	
Input Rise or Fall Times	$t_r, t_f$	$V_{CC} = 2V$	0	1000	ns
		$V_{CC} = 4.5V$	0	500	
		$V_{CC} = 6.0V$	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	$V_{CC}$	CONDITIONS	LIMITS			UNITS
				25 $^{\circ}C$	85 $^{\circ}C$	FULL RANGE <sup>4</sup>	
Minimum High-Level Input Voltage	$V_{IH}$	2.0V	$V_{OUT} = V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	1.5	1.5	1.5	V
		3.0V		2.1	2.1	2.1	
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	$V_{IL}$	2.0V	$V_{OUT} = V_{CC} - 0.1V$ $ I_{OUT}  \leq 20\mu A$	0.5	0.5	0.5	V
		3.0V		0.9	0.9	0.9	
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

4. -55 $^{\circ}C \leq T_J \leq +125^{\circ}C$





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## DC Electrical Characteristics continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Minimum High-Level Output Voltage	V <sub>OH</sub>	2.0V	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20μA	1.9	1.9	1.9	V
		4.5V		4.4	4.4	4.4	
		6.0V		5.9	5.9	5.9	
		3.0V	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 3.6mA	2.48	2.34	2.2	V
		4.5V		3.98	3.84	3.70	
		6.0V		5.48	5.34	5.20	
Maximum Low-Level Output Voltage	V <sub>OL</sub>	2.0V	V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20μA	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		3.0V	V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 3.6mA	0.26	0.33	0.40	V
		4.5V		0.26	0.33	0.40	
		6.0V		0.26	0.33	0.40	
Maximum Input Leakage Current	I <sub>IN</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND	±0.1	±1.0	±1.0	μA
Maximum 3-State leakage current	I <sub>OZ</sub>	6.0V	V <sub>OUT</sub> = V <sub>CC</sub> or GND, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	±0.5	±5.0	±10	μA
Maximum Quiescent Supply Leakage Current	I <sub>CC</sub>	6.0V	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0μA	4	40	160	μA

## AC Electrical Characteristics<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Input A to Output Y (Figure 1, 3)	t <sub>PLH</sub> , t <sub>PHL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	90	115	135	ns
		3.0V		36	45	60	
		4.5V		18	23	27	
		6.0V		15	20	23	
Maximum Propagation Delay, Output Enable to Y (Figure 2,4)	t <sub>PLZ</sub> , t <sub>PHZ</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	120	150	180	ns
		3.0V		45	60	80	
		4.5V		24	30	36	
		6.0V		20	26	31	





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## AC Electrical Characteristics continued<sup>5</sup>

PARAMETER	SYMBOL	V <sub>CC</sub>	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE <sup>4</sup>	
Maximum Propagation Delay, Output Enable to Y (Figure 2,4)	t <sub>PZL</sub> , t <sub>PZH</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	90	115	135	ns
		3.0V		36	45	60	
		4.5V		18	23	27	
		6.0V		15	20	23	
Maximum Output Rise and Fall Time (Figure 1, 3)	t <sub>TLH</sub> , t <sub>THL</sub>	2.0V	C <sub>L</sub> = 50pF, Input t <sub>r</sub> = t <sub>f</sub> = 6ns	60	75	90	ns
		3.0V		22	28	34	
		4.5V		12	15	18	
		6.0V		10	13	15	
Maximum Input Capacitance	C <sub>IN</sub>	-	-	10	10	10	pF
Maximum Three-State Output Capacitance (Output in High-Z)	C <sub>OUT</sub>	-	-	15	15	15	pF
Power Dissipation Capacitance (Per Buffer) <sup>5</sup>	C <sub>PD</sub>	-	T <sub>J</sub> = 25°C, V <sub>CC</sub> = 5.0V	TYPICAL			pF
				30			

5. Not production tested in die form, characterized by chip design and tested in package LAT.

6. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## Switching Waveforms

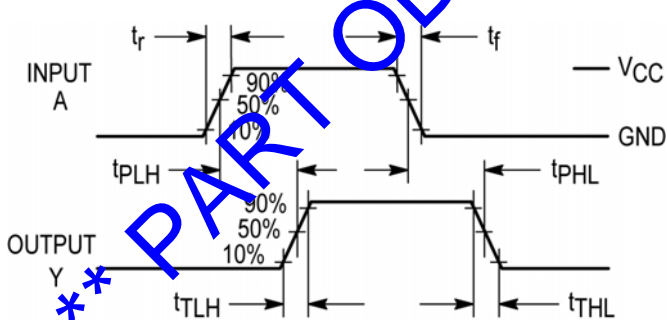


Figure 1 – Propagation Delay & Output Transition Time

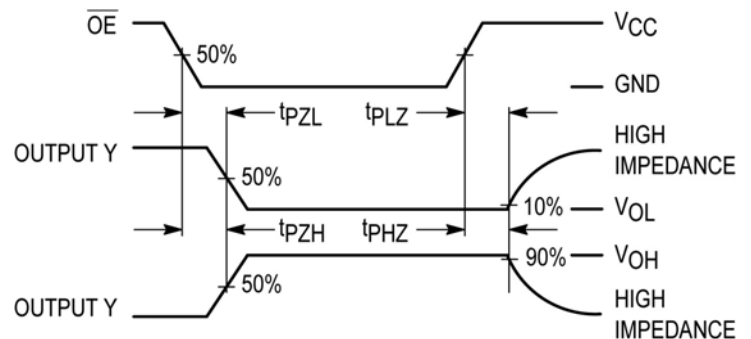


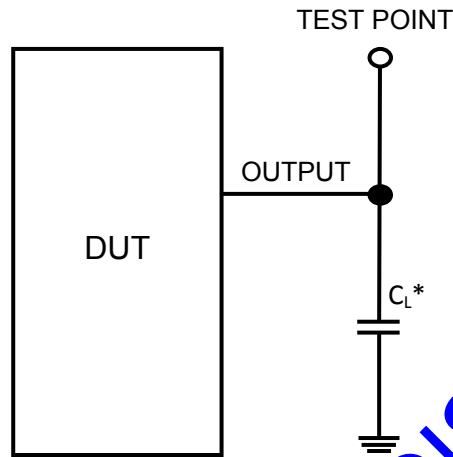
Figure 2 – Propagation Delay & Output Transition Time





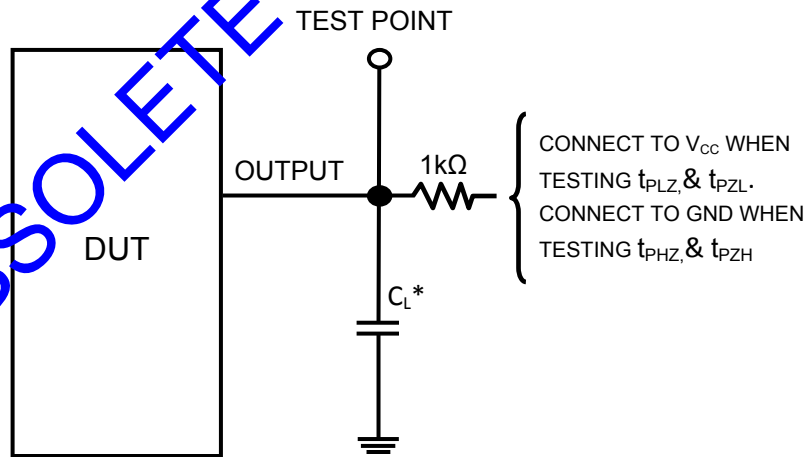
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## Test Circuits



\* Includes all probe and jig capacitance

Figure 3



\* Includes all probe and jig capacitance

Figure 4

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