High Speed CMOS Logic – 54HC05

Hex Inverter Gate with Open-Drain Outputs in bare die form

Rev 1.0
22/04/19

Description

The 54HC05 hex inverter gate is fabricated on a 2.5µm 5V CMOS process combining high speed LSTTL performance with CMOS low power. The device contains six independent inverters with open-drain outputs and perform the Boolean function Y = Ā . Device outputs can connect with other open-drain outputs to form active LOW wired-OR or active HIGH wired-AND logic functions. Open-drain outputs need pull-up resistors to perform correctly*. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

Features:

- Output Drive Capability: 10 LSTTL Loads*
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 54LS05
- High Noise Immunity CMOS process
- Full Military Temperature Range.

Ordering Information

The following part suffixes apply:

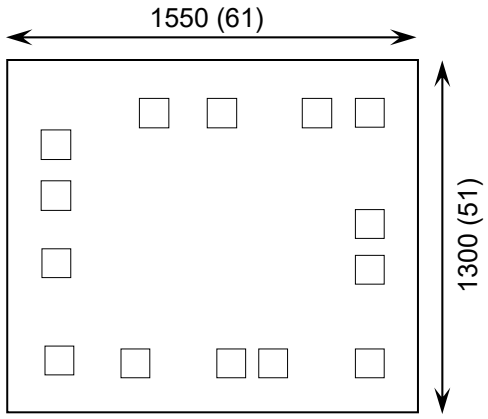
- No suffix - MIL-STD-883 /2010B Visual Inspection
- "**H**" - MIL-STD-883 /2010B Visual Inspection
  + MIL-PRF-38534 Class H LAT
- "**K**" - MIL-STD-883 /2010A Visual Inspection (Space)
  + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Die Dimensions in µm (mils)



Supply Formats:

- Default – Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape – On request
- Unsawn Wafer – On request
- Die Thickness <> 350µm(14 Mils) – On request
- Assembled into Ceramic Package – On request

Mechanical Specification

Die Size (Unsawn)	1550 x 1300 61 x 51	µm mils
Minimum Bond Pad Size	106 x 106 4.17 x 4.17	µm mils
Die Thickness	350 (±20) 13.78 (±0.79)	µm mils
Top Metal Composition	Al 1%Si 1.1µm	
Back Metal Composition	N/A – Bare Si	

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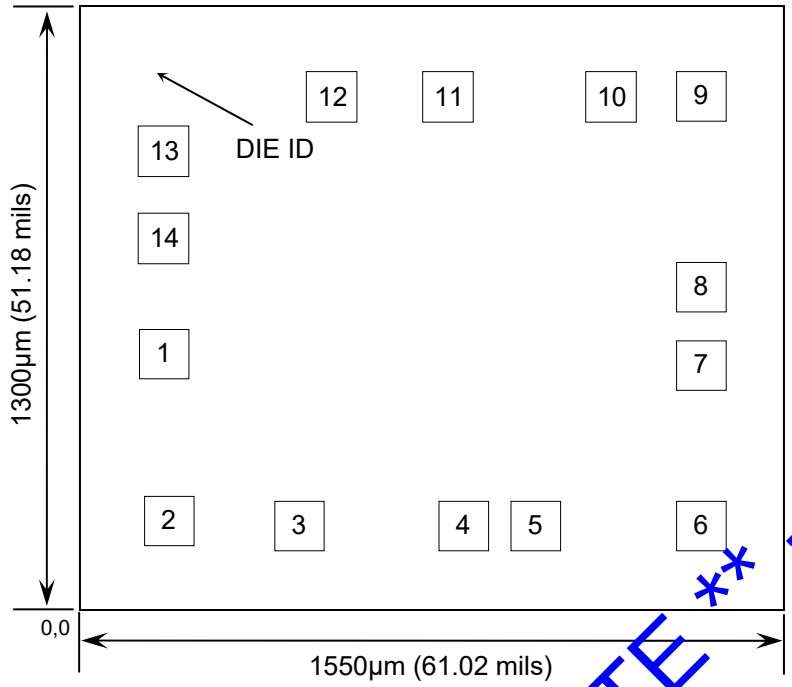
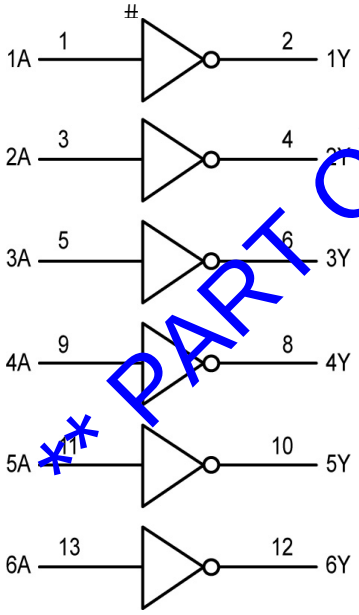
Pad Layout and Functions



PAD	FUNCTION	COORDINATES (µm)	
		X	Y
1	1A	126	492
2	1Y	136	122
3	2A	432	112
4	2Y	793	112
5	3A	948	112
6	3Y	1312	112
7	GND	1312	471
8	4Y	1312	643
9	4A	1312	1062
10	5Y	1107	1062
11	5A	747	1062
12	6Y	492	1062
13	6A	126	941
14	V_{CC}	126	747
CONNECT CHIP BACK TO V_{CC} OR FLOAT			

Logic Diagram



Pad 14 = V_{CC}
Pad 7 = GND

Truth Table

INPUTS A	OUTPUT Y
H	L
L	Z

H = High level (steady state)
L = Low level (steady state)
Z = High-impedance off-state

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Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to +150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN} ,V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-55	+125	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6.0V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Minimum High-Level Input Voltage	V_{IH}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	1.5	1.5	1.5	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage	V_{IL}	2.0V	V_{OUT} = 0.1V or V_{CC} -0.1V $\lvert I_{OUT} \rvert$ ≤ 20µA	0.5	0.5	0.5	V
		4.5V		1.35	1.35	1.35	
		6.0V		1.8	1.8	1.8	

4. -55˚C ≤ T_J ≤ +125˚C

DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Low-Level Output Voltage	V_{OL}	2.0V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 20\mu A$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V		0.1	0.1	0.1	
		4.5V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 4.0mA$	0.26	0.33	0.40	
		6.0V	$V_{IN} = V_{IL}$ or V_{IL} $\lvert I_{OUT} \rvert \leq 5.2mA$	0.26	0.33	0.40	
Maximum Input Leakage Current	I_{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	µA
Maximum Quiescent Supply Leakage Current	I_{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	40	µA
Maximum Three-State Leakage Current	I_{OZ}	6.0V	Output in high impedance state, $V_{IN} = V_{IL}$ or V_{IH} $V_{OUT} = V_{CC}$ or GND	±0.5	±5	±10	µA

AC Electrical Characteristics[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Propagation Delay, Input A or B to Output Y (Figure 1,2)	t_{PLH}, t_{PHL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	90	115	135	ns
		4.5V		18	23	27	
		6.0V		15	20	23	
Maximum Output Transition Time, Any Output (Figure 1,2)	t_{THL}	2.0V	$C_L = 50pF$, Input $t_r = t_f = 6ns$	75	95	110	ns
		4.5V		15	19	22	
		6.0V		13	16	19	

Capacitance[5]

PARAMETER	SYMBOL	V_{CC}	CONDITIONS	LIMITS			UNITS
				25°C	85°C	FULL RANGE[4]	
Maximum Input Capacitance	C_{IN}	6.0V	-	10	10	10	pF
Maximum Three-State Output Capacitance	C_{OUT}	6.0V	-	10	10	10	pF
Power Dissipation Capacitance Per Buffer[6]	C_{PD}	5.0V	$T_J = 25°C$, $V_{EE} = 0V$	TYPICAL			pF
				4			

5. Not production tested in die form, characterized by chip design and tested in package.
6. Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Typical Characteristics

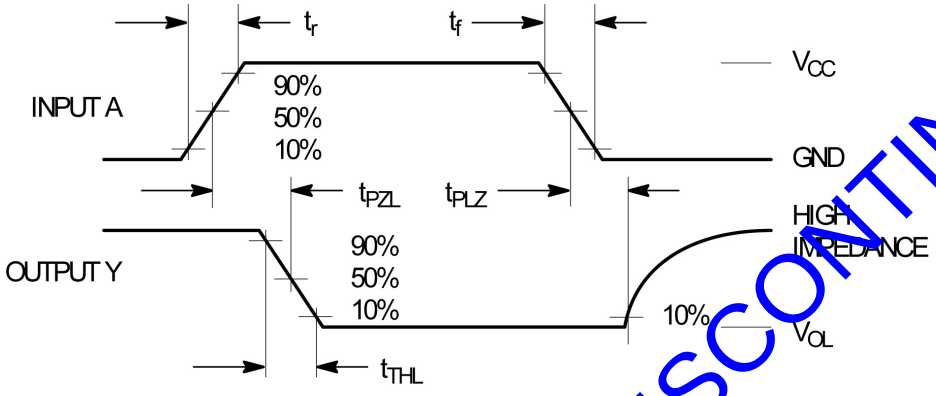
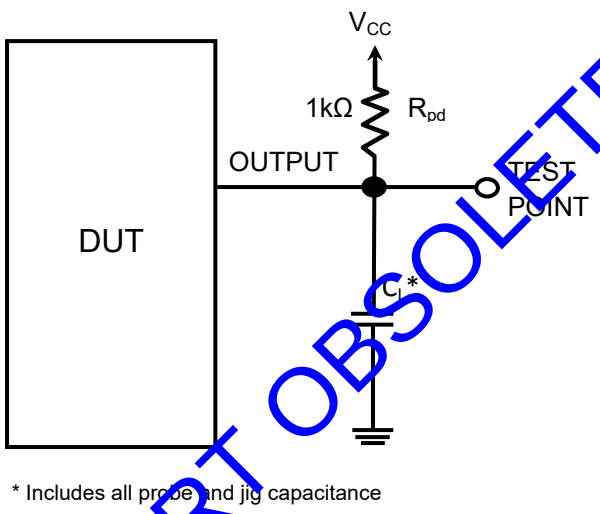


Figure 1 – Propagation Delay & Output Transition Time



* Includes all probe and jig capacitance

Figure 2 - Test Circuit

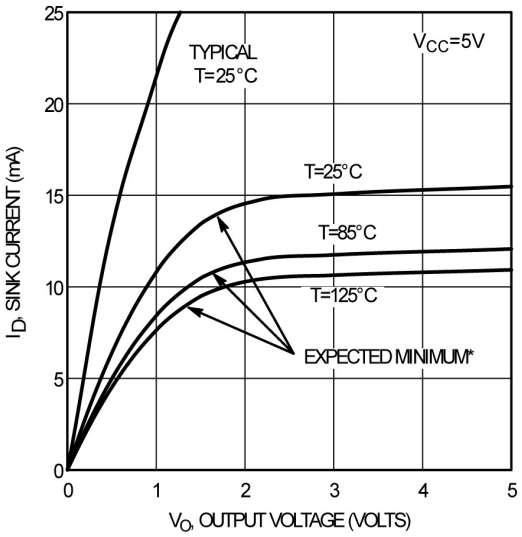


Figure 3 – Open-Drain Output Characteristics